25UMGT301	FOURIER TRANSFORMS AND COMPLEX ANALYSIS	Category	L	T	P	R	Credit	Year of Introduction
		BSC	3	0	0	0	3	2025

Preamble: This course introduces basic ideas of Fourier transforms which are widely used in the modelling and analysis of a wide range of physical phenomena and has got application across all branches of engineering. To understand the basic theory of functions of a complex variable, residue integration and conformal transformation.

Prerequisite: Nil

Course Outcomes: After the completion of the course, the student will be able to:

CO	Course Outcomes	Knowledge Level
CO1	Determine the Fourier transforms of functions and apply them to solve problems arising in engineering.	K3 Apply
CO2	Explain the analyticity of complex functions and apply it in Conformal mapping.	K3 Apply
CO3	Compute complex integrals using Cauchy's integral theorem and Cauchy's integral formula.	K3 Apply
CO4	Explain the series expansion of complex function about a singularity and apply residue theorem to compute real integrals.	K3 Apply

Mapping of course outcomes with program outcomes and program specific outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	3	3	2	2	-	-	-	-	-	-	1
CO2	3	3	2	2	-	-	-	-	-	-	1
CO3	3	3	2	2	-	-	-	-	-	-	1
CO4	3	3	2	2	-	-	-	-	-	-	1
Avg	3	3	2	2	-	-	-	-	-	-	1

Mapping of course outcomes with Knowledge and Attitude Profile (WK)

	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	*	*	*	*	*			*	
CO2	*	*	*	*	*			*	
CO3	*	*	*	*	*			*	
CO4	*	*	*	*	*			*	

WKs Mapped with the course

WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
*	*	*	*	*			*	

Mark Distribution:

Total Marks	CIE Marks	ESE Marks	ESE Duration
100	40	60	2.5 hrs

Continuous Internal Evaluation Pattern:

Attendance : 5 marks
Continuous Assessment Test : 20 marks
Continuous Assessment Assignment : 15 marks

SYLLABUS

Module 1 (10hrs)

Fourier integral, from Fourier series to Fourier integral Fourier cosine and and Sine integrals, Fourier Cosine and Sine Transform, Linearity, Transforms of Derivatives, Fourier Transform and its inverse, Linearity, Transforms of Derivative.

Module 2 (10hrs)

Complex Function, Limit, Continuity, Derivative, Analytic functions, Cauchy-Riemann Equations (without proof), Laplace's Equations, Harmonic functions, Finding harmonic conjugate, Conformal mapping, Mappings of $w=z^2$, $w=e^z$, w=, $w=sinz$.

Module 3 (11hrs)

Complex Integration: Line integrals in the complex plane (Definition & Basic properties), First evaluation method, Second evaluation method, Cauchy's integral theorem (without proof) on simply connected domain, Independence of path, Cauchy integral theorem on multiply connected domain (without proof), Cauchy Integral formula (without proof).

Module 4 (11hrs)

Taylor series and Maclaurin series, Laurent series (without proof), Singularities and Zeros – Isolated Singularity, Poles, Essential Singularities, Removable singularities, Zeros of Analytic functions – Poles and Zeros, Formulas for Residues, Residue theorem (without proof), Residue Integration- Integral of Rational Functions of $cos\theta$ and $sin\theta$.

Textbook

1.Kreyszig, E. (2016). *Advanced engineering mathematics* (10th ed.). John Wiley & Sons.

Reference Books

1. Zill, D. G., & Shanahan, P. D. (2015). *Complex analysis: A first course with applications* (3rd ed.). Jones & Bartlett Learning.

2. Ramana, B. V. (2023). *Higher engineering mathematics* (39th ed.). McGraw-Hill Education.

3. Grewal, B. S. (2018). *Higher engineering mathematics* (44th ed.). Khanna Publishers.

SEMESTER EXAMINATION - MODEL QUESTION PAPER

Course Code	**25UMBT301**
Course Name	**FOURIER TRANSFORMS AND COMPLEX ANALYSIS**
Max. Marks: 60	**Duration: 2.5 Hours**

Part A *(Answer all questions. Each question carries 3 marks)*	

Qn No.	Question	Marks	CO	BL
1	Find the Fourier cosine integral of f(x)=	3	1	L2
2	Find the Fourier transform of f(x)=	3	1	L2
3	Show that the function f(z)= does not have a limit as z=0	3	2	L3
4	Check whether the function u(x ,y) = is the real art of an analytic function.	3	2	L3
5	Evaluate where c is the line segment joining -i and i	3	3	L3
6	Evaluate where c is the unit circle	3	3	L3
7	Find the Taylor series expansion of f(z)= sin z about z=	3	4	L2
8	Find pole and residue of	3	4	L2
Part B (*Answer any one full question from each Module. Each carries 9 marks*)				
Module 1				
Qn No.	Question	Marks	CO	BL
7(a)	Find the Fourier cosine integral of the function f(x)= ,x>0 and hence show that	5	1	L3
(b)	Find the Fourier sine transform of the function f(x)=	4	1	L2
OR				
8(a)	Find the Fourier transform of f(x)=	5	1	L3
(b)	Find the Fourier sine integral of f(x)=	4	1	L2
MODULE-2				
9(a)	Show that f(z)= is differentiable everywhere. and find its derivative	5	2	L2
(b)	Show that u= is harmonic. and hence find the analytic function and harmonic conjugate	4	2	L3
OR				
10(a)	Find the analytic function whose imaginary part is	5	2	L2
(b)	Find the image of the infinite strip	4	2	L3
MODULE-3				
11(a)	Solve f(z)= from A(1,1) to B(2,4) along the curve x=t and	5	3	L3

	y=t			
(b)	Solve where c is $\|z+1-i\| = 2$	4	3	L3
OR				
12(a)	Solve where c is $\|z- i\|= 2$	5	3	L3
(b)	Solve where c is a straight line from 0 to (1+2i)	4	3	L3
MODULE-4				
13(a)	Expand f(z)= as a Taylor series about z= -1	5	4	L3
(b)	Find poles and residue of f(z)=	4	4	L2
OR				
14(a)	Solve where c is $\|z\|=3$	5	4	L3
(b)	Expand f(z)= as Taylor series about z= 2	4	4	L2

****

25UECT301	SEMICONDUCTOR DEVICE TECHNOLOGY	Category	L	T	P	R	Credit	Year of Introduction
		PCC	3	1	0	0	4	2025

Preamble: This course provides a fundamental understanding of semiconductor materials and the operating principles of essential semiconductor devices used in modern electronic systems.

Prerequisite : PHYB102 Physics for Electrical Science

Course Outcomes: After the completion of the course, the student will be able to:

Course Outcomes		Knowledge Level
CO1	Apply semiconductor material properties and carrier transport principles to determine carrier behavior.	**K3 Apply**
CO2	Apply PN junction concepts to explain the operation and current mechanisms of bipolar junction transistors.	**K3 Apply**
CO3	Apply MOS capacitor concepts and MOSFET operation principles to analyze device characteristics.	**K3 Apply**
CO4	Apply concepts of scaling, short-channel effects, and advanced MOS devices in modern electronic systems.	**K3 Apply**

Mapping of course outcomes with program outcomes and program specific outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	2	-	2	-	-	-	-	-	-	2	3	2
CO2	3	3	-	2	-	-	-	-	-	-	2	3	2
CO3	2	3	2	2	2	-	-	-	-	-	3	3	3
CO4	2	3	2	3	2	-	-	-	-	-	3	3	3
Avg	2.5	2.75	2	2.25	2	-	-	-	-	-	2.5	3	2.5

Mapping of course outcomes with Knowledge and Attitude Profile (WK)

	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	*	*	*	*				*	
CO2	*	*	*	*				*	
CO3	*	*	*	*	*	*		*	
CO4	*	*	*	*	*	*		*	

WKs Mapped with the course

WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9

*	*	*	*	*	*		*	

Mark Distribution:

Total Marks	CIE Marks	ESE Marks	ESE Duration
100	40	60	2.5 hrs

Continuous Internal Evaluation Pattern:

Attendance : 5 marks

Continuous Assessment Test : 20 marks

Continuous Assessment Assignment : 15 marks

SYLLABUS

Module 1 (16 Hrs)

Semiconductor Basics and Carrier Transport: Elemental and compound semiconductors, intrinsic and extrinsic semiconductors, effective mass, Fermi Dirac distribution, Fermi level, energy band diagrams, equilibrium and steady-state conditions, Excess carriers in semiconductors: Generation and recombination mechanisms of excess carriers, quasi Fermi levels.

Carrier concentration: Drift and diffusion mechanisms, mobility, conductivity, Hall effect and overview of transport equations. Einstein relations, Poisson equations, Continuity equations, Current flow equations, Diffusion length, Gradient of quasi Fermi level

Module 2 (15 Hrs)

PN Junctions and Bipolar Devices: PN junction formation, contact potential, electric field, charge distribution, biasing and Energy band diagrams, and ideal diode equation and characteristics.

Metal–semiconductor contacts. Electron affinity and work function,

Ohmic and Rectifying Contacts.

Bipolar junction transistor: operation, current components and base width modulation

Module 3 (15 Hrs)

MOS Capacitor and MOSFET Operation: MOS capacitor behavior in accumulation, depletion and inversion, threshold voltage and body effect. MOSFET: structure and types, basic drain current equations, drain and transfer characteristics.

Module 4 (10 Hrs)

MOSFET Scaling and Advanced Devices: Scaling concepts, sub-threshold conduction and short-channel effects.

Introduction to advanced devices such as MESFET and FinFET.

Text Books

1. Streetman, B. G., & Banerjee, S. K. (2010). *Solid state electronic devices* (6th ed.). Pearson Education.
2. Kang, S. M., & Leblebici, Y. (2002). *CMOS digital integrated circuits: Analysis and design* (3rd ed.). McGraw-Hill.
3. Pierret, R. F. (1996). *Semiconductor device fundamentals*. Addison-Wesley (Pearson Education).

Reference Books

1. Neamen, D. A. (2012). *Semiconductor physics and devices* (4th ed.). McGraw-Hill.
2. Sze, S. M., & Lee, M.-K. (2005). *Semiconductor devices: Physics and technology* (3rd ed.). John Wiley & Sons.
3. Pierret, R. F. (2006). *Semiconductor device fundamentals*. Pearson Education.
4. Sze, S. M. (2005). *Physics of semiconductor devices* (3rd ed.). John Wiley & Sons.

END SEMESTER EXAMINATION – MODEL QUESTION PAPER

Course Code	**25UECT301**

Course Name	**SEMICONDUCTOR DEVICE TECHNOLOGY**
Max. Marks: 60	**Duration: 2.5 Hours**

Part A

(Answer all questions. Each question carries 3 marks)

Qn No.	Question	Marks	CO	BL
1	Differentiate drift and diffusion movement of carriers in semiconductors.	3	1	L2
2	A solar-powered calculator manufacturer finds that pure silicon has low electrical conductivity. To improve device performance, engineers add impurity atoms to the silicon crystal. Apply the concept of doping to show how an intrinsic semiconductor is converted into an extrinsic semiconductor and how its conductivity is improved.	3	1	L3
3	Explain electron affinity and work function.	3	2	L2
4	An amplifier circuit used in a communication system experiences variations in collector current when the collector-base voltage is increased, even though the base current is maintained constant. Apply the concept of the Early effect to illustrate why this occurs and explain its impact on the collector and base currents of the transistor.	3	2	L3
5	Explain the effect of real surfaces of a MOS capacitor.	3	3	L2
6	A power supply circuit uses a metal–n-type semiconductor junction to allow current flow in one direction while blocking it in the opposite direction. Apply the concept of a metal–semiconductor contact to illustrate the rectifying behaviour of the junction and explain how it controls current flow under forward and reverse bias conditions.	3	3	L3
7	Explain Drain induced barrier lowering.	3	4	L2

8	A semiconductor company is developing next-generation processors and requires transistors with better control over channel conduction and reduced leakage current than conventional MOSFETs. Illustrate how a FinFET structure addresses these requirements by drawing and explaining its structure and highlighting the role of the fin-shaped channel in improving device performance.	3	4	L3
Part B (*Answer any one full question from each Module. Each carry 9 marks*)				
Module I				
Qn No.	**Question**	**Marks**	**CO**	**BL**
9	Derive the expression for electron, hole and intrinsic concentrations at equilibrium in terms of effective density of states.	9	1	L3
OR				
10	Derive the expression for drift current density, mobility of carriers and conductivity of a semiconductor.	9	1	L3
Module II				
Qn No.	**Question**	**Marks**	**CO**	**BL**
11	Derive ideal diode equation with a neat sketch.	9	2	L3
OR				
12	Derive the expression for potential distribution of a PN junction at equilibrium.	9	2	L3
Module III				
Qn No.	**Question**	**Marks**	**CO**	**BL**
13. a	Derive the expression for drain current in linear and saturation region.	5	3	L3
13. b	In an electronics lab, engineers are testing an n-channel enhancement MOSFET used in an analog switching circuit.	4	3	L3

	During analysis, they observe how the drain current varies with gate-source voltage in both linear and saturation regions. Apply this behaviour to illustrate the transfer characteristics of the MOSFET and show how it changes across linear and saturation regions.			
	OR			
14. a	A silicon-based MOS capacitor used in a microelectronic sensor has a p-type substrate with doping concentration $N_A=10^{15}cm^{-3}$ and a gate oxide thickness of 100 Å. The device is operated at the onset of strong inversion for analysis of its switching behaviour. Determine: (i) Width of the depletion layer. (ii) Charge density in the depletion layer. (iii) Threshold voltage. Given $\varepsilon_{rox}=3.9,\varepsilon_{rsi}=11.8$.	5	3	L3
14. b	A silicon n-channel MOSFET used in an analog signal processing circuit is designed with an n polysilicon gate and is operated under the conditions V_{GS} = 3 V, V_{DS} = 5V, V_T = 0.76 V, t_{ox} = 300A^0, μ_n = 600 cm^2/Vs, z = 50 μm, L = 10 μm, and C_{ox} = 1.15 x 10^{-7} F/cm^2. Apply MOSFET current equations to determine the drain current under the given operating conditions.	4	3	L3
	Module IV			
Qn No.	**Question**	**Marks**	**CO**	**BL**
15. a	A short-channel MOSFET used in a VLSI high-speed circuit shows performance degradation when operated at high drain voltage due to high-energy carriers near the drain region. Apply the concept of hot carrier effect to explain its impact on the performance and reliability of a short-channel MOSFET.	6	4	L3
15. b	A high-frequency communication system uses MESFET	3	4	L3

	devices to achieve faster signal processing compared to conventional transistors. Engineers analyze its device behaviour to understand why it is suitable for microwave applications. Apply the concept of MESFET to explain its principle of operation, structure, and advantages in high-frequency applications.			
	OR			
16. a	A MOSFET fabrication process is being optimized in semiconductor technology where device scaling is required to improve speed and packing density, and engineers compare constant field scaling with constant voltage scaling to understand their impact on device performance and reliability. Apply the concept of constant field scaling to explain its principle and its advantages over constant voltage scaling.	6	4	L3
16. b	A MOSFET used in an analog integrated circuit shows a slight increase in drain current even after the device enters saturation, affecting the accuracy of circuit operation. Apply the concept of channel length modulation to explain its effect on the drain characteristics of the MOSFET.	3	4	L3

25UECT302	ELECTRONIC CIRCUITS - I	Category	L	T	P	R	Credit	Year of Introduction
		PCC	3	1	0	0	4	2025

Preamble: This course develops fundamental knowledge of electronic devices and circuits, focusing on their principles of operation, analysis, and practical applications. It enables students to understand circuit behavior, evaluate performance characteristics, and apply electronic systems in engineering practice.

Prerequisite: IEE 104 Introduction to Electrical and Electronics Engineering

Course Outcomes: After the completion of the course, the student will be able to:

CO	Course Outcomes	Knowledge Level
CO1	Apply biasing concepts to analyze BJT and MOSFET circuits and	K3

	design linear and non-linear wave shaping circuits.	Apply
CO2	Perform small-signal analysis of BJT and MOSFET amplifiers using hybrid-π models.	K3 Apply
CO3	Apply feedback principles to analyze amplifier topologies and determine operating conditions of sinusoidal oscillators.	K3 Apply
CO4	Apply design principles to analyze power amplifiers and linear voltage regulators.	K3 Apply

Mapping of course outcomes with program outcomes and program specific outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	**3**	**3**	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**2**	**3**	**3**
CO2	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**2**	**3**	**2**
CO3	**3**	**3**	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**3**	**3**	**3**
CO4	**3**	**3**	**3**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**3**	**3**	**3**
Avg	**3**	**3**	**2.75**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**2.5**	**3**	**2.75**

Mapping of Course Outcomes with Knowledge and Attitude Profile (WK)

	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	*	*	*	*	*	*		*	
CO2	*	*	*	*	*	*		*	
CO3	*	*	*	*	*	*		*	
CO4	*	*	*	*	*	*		*	

WKs Mapped with the Course

WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
*	*	*	*	*	*		*	

Mark Distribution:

Total Marks	CIE Marks	ESE Marks	ESE Duration
100	**40**	**60**	**2.5 hrs**

Continuous Internal Evaluation Pattern:

Attendance : 5 marks
Continuous Assessment Test : 20 marks
Continuous Assessment Assignment/Industrial Visit/Training Report : 15 marks

SYLLABUS

Module 1 (14 hrs)

Linear and Non-Linear Wave Shaping Circuits: RC differentiating and integrating circuits, Analysis of First order RC low pass and high pass filters. Positive, negative and biased Diode Clipping and Clamping circuits.
Transistor Biasing: Need for biasing, bias stabilization, concept of AC and DC load lines, operating point, stability factor, BJT and MOSFET biasing circuits.

Module 2 (14 hrs)
Design of BJT RC-coupled CE amplifier with frequency response, Small-signal analysis using hybrid-π model for mid-frequency and low-frequency regions. High-frequency BJT equivalent circuits and Miller effect. Multistage BJT amplifiers, effect of cascading on overall gain and bandwidth, and Small-signal evaluation of the BJT cascode amplifier employing the hybrid-π model. Design of the MOSFET CS amplifier and its mid-frequency small-signal analysis using the hybrid-π model, including CS stage with current-source load and diode-connected load.

Module 3 (14 hrs)
General feedback configuration of feedback amplifiers, effect of negative and positive feedback on gain, bandwidth, noise, and distortion. Feedback topologies and analysis of discrete BJT circuits under voltage-series and voltage-shunt feedback.
Classification and conditions for oscillation in Sinusoidal oscillators, operating principles and design relations of Hartley and Crystal oscillators, and analysis of the Wien bridge oscillator.

Module 4 (14 hrs)
Classification of Power amplifiers, transformer-coupled Class A amplifier, push-pull Class B and Class AB amplifiers, complementary symmetry Class B and Class AB amplifiers with efficiency and distortion considerations. Series and shunt Linear voltage regulators, operation and design aspects, load and line regulation, short-circuit protection, and foldback current limiting.

An industrial visit or short-term training program in a reputed Electronics and Communication Engineering industry or organization to provide students with practical exposure to real-world engineering practices is highly appreciable.

Text Books:

1. Boylestad, R. L., & Nashelsky, L. (2019). *Electronic devices and circuit theory* (12th ed.). Pearson.

2. Sedra, A. S., Smith, K. C., Carusone, A. C., & Gaudet, V. (2020). *Microelectronic circuits* (8th ed.). Oxford University Press.

3. Bogart, T. F., Beasley, J. S., & Rico, G. (2019). *Electronic devices and circuits* (7th ed.). Pearson.

Reference Books:

1. Razavi, B. (2015). *Fundamentals of microelectronics* (2nd ed.). Wiley.

2. Bell, D. A. (2008). *Electronic devices and circuits* (5th ed.). Oxford University Press.

3. Gopakumar, K. (2023). *Analysis and design of electronic circuits* (1st ed.). OWL Books.

END SEMESTER EXAMINATION – MODEL QUESTION PAPER

Course Code	**25UECT302**
Course Name	**ELECTRONIC CIRCUITS - I**
Max. Marks: 60	**Duration: 2.5 Hours**

Part A
(Answer all questions. Each question carries 3 marks)

Qn No.	Question	Marks	CO	BL
1.	A fixed-bias network is used to establish the operating point of a transistor amplifier. Describe the operation of the circuit and explain the limitations that affect its practical use.	3	1	L2
1.	A signal-conditioning circuit requires an op-amp integrator to process a 20 V peak-to-peak square wave of frequency 1.5 kHz. Design the integrator circuit by selecting suitable values of R and C, and verify that the chosen components satisfy the condition for proper integration.	3	1	L3
1.	Describe the Miller effect in transistor amplifiers and explain its significance on the high-frequency performance of amplifiers.	3	2	L2
1.	A multistage audio amplifier employs RC coupling to achieve the desired gain. With a neat circuit diagram, determine the contribution of each component to the overall operation of the amplifier and show the signal flow between stages.	3	2	L3
1.	A feedback oscillator is designed to generate a stable output waveform. Describe the Barkhausen criteria and discuss how these conditions ensure sustained oscillations.	3	3	L2
1.	A voltage-series negative feedback amplifier is used in an audio signal amplifier to improve stability and impedance characteristics. The amplifier has an open-loop voltage gain of A = 500, input resistance of 3kΩ, output resistance of 20kΩ, and feedback factor β = 0.01. Calculate the closed-loop voltage gain A_f, input resistance with feedback R_{if}, and output resistance with feedback R_{of}.	3	3	L3
1.	An audio power amplifier is designed to provide efficient amplification with improved output quality. Describe the characteristics of Class AB operation that make it suitable for	3	4	L2

	practical amplifier applications.			
1.	A regulated DC power supply operates under varying input voltage and load conditions. Determine the line regulation and load regulation characteristics of the power supply, and illustrate their significance in maintaining a stable output voltage.	3	4	L3
Part B (*Answer any one full question from each Module. Each carry 9 marks*)				
Module I				
Qn No.	**Question**	**Marks**	**CO**	**BL**
1.	A signal-processing circuit requires a sine-wave input to be restricted within the voltage limits of +3 V and −4 V. Design a suitable slicer circuit using ideal diodes and determine the resulting output waveform and transfer characteristics.	9	1	L3
OR				
1.	An RC differentiator is used in a wave-shaping circuit to produce output pulses corresponding to sudden changes in the input waveform. Derive the design equation and show that the output voltage is proportional to the rate of change of the input voltage.	9	1	L3
Module II				
Qn No.	**Question**	**Marks**	**CO**	**BL**
1.	A transistor amplifier is required to provide voltage amplification in the mid-frequency range. Using the hybrid-π small-signal model, determine the expressions for the input impedance, output impedance, and mid-band voltage gain of the common-emitter amplifier.	9	2	L3
OR				
1.	A MOSFET common-source amplifier uses a diode-connected load to obtain voltage amplification in an integrated circuit. Using the small-signal model, derive the expressions for voltage gain, input resistance, and output resistance of the common-source amplifier with diode-connected load.	9	2	L3
Module III				
Qn No.	**Question**	**Marks**	**CO**	**BL**
13. a	A feedback network is introduced in an amplifier to improve overall performance. Determine how negative feedback affects gain, bandwidth, stability, and distortion in the amplifier.	4	3	L3
13. b	A Wien bridge oscillator is used to generate a stable sinusoidal waveform in an audio-frequency signal generator. Draw its circuit and derive the expression for the frequency of oscillation.	5	3	L3
OR				
14.				

a	A voltage amplifier uses voltage-series negative feedback to improve its input and output impedance characteristics. Draw the block diagram of voltage-series feedback topology and derive the expressions for net input impedance and output impedance.	5	3	L3
14. b	A crystal oscillator is used in a communication system to generate a highly stable frequency reference. With the necessary circuit diagram, illustrate the operation of the crystal oscillator and show the role of the crystal in frequency stabilization.	4	3	L3
Module IV				
Qn No.	**Question**	**Marks**	**CO**	**BL**
15. a	A DC power supply is required to maintain a constant output voltage even when the load current varies. With the necessary circuit diagram, illustrate the working of a shunt voltage regulator.	4	4	L3
15. b	A Class B audio amplifier delivers a 20 V peak output signal to a 16 Ω speaker using a 30 V DC supply. Determine the input power, output power, and circuit efficiency of the amplifier.	5	4	L3
OR				
16. a	An audio output stage uses a complementary pair of transistors to drive a speaker load efficiently. Draw the circuit of a complementary-symmetry push-pull amplifier and illustrate its working.	4	4	L3
16. b	A complementary-symmetry Class B push-pull power amplifier operates with supply voltages of +12V and −12V and drives an 8Ω load. Calculate the maximum input power, maximum output power, and maximum efficiency of the amplifier.	5	4	L3

25UECT303	**DIGITAL LOGIC DESIGN**	**Category**	**L**	**T**	**P**	**R**	**Credit**	**Year of Introduction**
		PBL	**3**	**1**	**0**	**1**	**4**	**2025**

Preamble: This course provides a strong foundation in digital electronics and digital system design, covering number systems, Boolean algebra, logic gates, and Karnaugh map simplification techniques. It focuses on the design and analysis of combinational and sequential circuits using standard digital components and finite state machine models. The course also introduces Verilog HDL for hardware modeling and implementation, and discusses logic families such as TTL, ECL, and CMOS with their characteristics and performance. Overall, it develops students' analytical, design, and practical skills for modern digital and embedded system applications..

Prerequisite: Nil

Course Outcomes: After the completion of the course, the student will be able to:

CO	Course Outcomes	Knowledge Level
CO1	Apply the knowledge of digital representation of information and Boolean algebra to deduce optimal digital circuits.	K3 Apply
CO2	Apply the principles of digital logic to construct combinational circuits such as adders, subtractors, multiplexers, decoders, and encoders.	K3 Apply
CO3	Apply the concepts of synchronous sequential circuits and finite state machines to solve complex digital system problems.	K3 Apply
CO4	Apply Verilog HDL to implement digital circuits and examine the characteristics of different logic families based on their electrical and performance parameters.	K3 Apply

Mapping of course outcomes with program outcomes and program specific outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	2	2	1	1	-	-	-	1	1	2	3	1
CO2	3	3	3	2	2	-	-	-	1	1	2	3	2
CO3	3	3	3	2	2	-	-	-	2	1	2	3	2
CO4	3	2	2	2	3	-	-	-	2	2	3	3	3
Avg	3.0	2.5	2.5	1.75	2.0	-	-	-	1.5	1.25	2.25	3.0	2.0

Mapping of course outcomes with Knowledge and Attitude Profile (WK)

	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	*	*	*	*	*	*		*	
CO2	*	*	*	*	*	*		*	
CO3	*	*	*	*	*	*		*	
CO4	*	*	*	*	*	*		*	

WKs Mapped with the course

WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
*	*	*	*	*	*		*	

Mark Distribution:

Total Marks	CIE Marks	ESE Marks	ESE Duration
100	60	40	2.5 hrs

Continuous Internal Evaluation Pattern:

Attendance : 5 marks
Continuous Assessment Test : 25 marks
Project : 30 marks

Assessment and Evaluation for Project Activity

Sl. No	Evaluation for	Allotted Marks
1	Project Planning and Proposal	5
2	Contribution in Progress Presentations and Question Answer Sessions	4
3	Involvement in the project work and Team Work	3
4	Execution and Implementation	10
5	Final Presentations	5
6	Project Quality, Innovation and Creativity	3
	Total	30

Project Assessment and Evaluation criteria (30 Marks)

1. Project Planning and Proposal (5 Marks)
   - Clarity and feasibility of the project plan
   - Research and background understanding
   - Defined objectives and methodology
2. Contribution in Progress Presentation and Question Answer Sessions (4 Marks)

   Individual contribution to the presentation

   Effectiveness in answering questions and handling feedback

3. Involvement in the Project Work and Team Work (3 Marks)
   - Active participation and individual contribution
   - Teamwork and collaboration

4. Execution and Implementation (10 Marks)
Adherence to the project timeline and milestones
Application of theoretical knowledge and problem-solving
Final Result

5. Final Presentation (5 Marks)
    Quality and clarity of the overall presentation
    Individual contribution to the presentation
    Effectiveness in answering questions
6. Project Quality, Innovation, and Creativity (3 Marks)
    Overall quality and technical excellence of the project
    Innovation and originality in the project
    Creativity in solutions and approaches

SYLLABUS

Module 1 (14 hrs)

Number Systems — Decimal, Binary, Octal, Hexadecimal, 1's and 2's complements, Codes — Binary, BCD, Excess 3, Gray, Alphanumeric codes, Boolean theorems, Logic gates, Universal gates, Sum of products and product of sums, Minterms and Maxterms, Karnaugh map Minimization

Module 2 (14 hrs)

Design of Half and Full Adders, Half and Full Subtractors, Binary Parallel Adder — Carry look ahead Adder, BCD Adder, Multiplexer, Demultiplexer, Magnitude Comparator, Decoder, Encoder, Priority Encoder.

Module 3 (14 hrs)

Flip flops — SR, JK, T, D, Master/Slave FF — operation and excitation tables, Triggering of FF, Analysis and design of clocked sequential circuits — Design — Moore/Mealy models, state minimization, state assignment, circuit implementation — Design of Counters- Ripple Counters, Ring Counters, Shift registers, Universal Shift Register.

Module 4 (14 hrs)

Introduction to Verilog HDL – Basic language elements, Basic implementation of logic gates and combinational circuits.
Logic Families: -Electrical characteristics of logic gates (Noise margin, Fan- in, Fan-out, Propagation delay, Transition time, Power -delay product) -TTL, ECL, CMOS. Circuit description and working of TTL and CMOS inverter, CMOS NAND and CMOS NOR gates.

Text Books:

1. M. M. Mano, *Digital Logic and Computer Design*, 4th ed. Noida, India: Pearson Education, 2013.
2. T. L. Floyd, *Digital Fundamentals*, 10th ed. Noida, India: Pearson Education, 2009.
3. S. Palnitkar, *Verilog HDL: A Guide to Digital Design and Synthesis*, 2nd ed. Noida, India: Pearson Education, 2003.

.

Reference Books:

1. M. M. Mano and M. D. Ciletti, *Digital Design with an Introduction to the Verilog HDL*, 5th ed. Noida, India: Pearson Education, 2013.
2. D. D. Givone, *Digital Principles and Design*. New Delhi, India: Tata McGraw-Hill, 2003.
3.J. F. Wakerly, *Digital Design: Principles and Practices*, 5th ed. Noida, India: Pearson Education, 2018.
4. A. Ananthakumar, *Fundamentals of Digital Circuits*, 4th ed. New Delhi, India: PHI Learning, 2016.

END SEMESTER EXAMINATION – MODEL QUESTION PAPER

Course Code	**25UECT303**
Course Name	**DIGITAL LOGIC DESIGN**
Max. Marks: 40	**Duration: 2.5 Hours**

Part A
(Answer all questions. Each question carries 2 marks)

Qn No.	Question	Marks	CO	BL
1	Convert (245.75) to Binary, Octal, and Hexadecimal.	2	CO1	L2
2	State and prove De Morgan's theorems with truth table verification.	2	CO1	L2
3	Express the Boolean function F(A,B,C) = Σm(1,3,5,7) in canonical Sum of Products (SOP) form and simplify using K-map.	2	CO1	L3
4	Design a half adder. Write the truth table and derive the logic expressions.	2	CO2	L3
5	Explain the operation of a JK Master-Slave Flip-Flop with a neat circuit diagram and timing diagram.	2	CO3	L2
6	Draw and explain a 4-bit ring counter using D flip-flops. Write the state sequence.	2	CO3	L2
7	Write a Verilog HDL module for a 2-to-1 multiplexer using data flow modelling.	2	CO4	L2
8	Define Fan-in, Fan-out and Noise Margin of logic gates. Why are these parameters important?	2	CO4	L2

Part B
(Answer any one full question from each Module. Each carries 6 marks)

Qn No.	Question	Marks	CO	BL
Module I				
9	a) Perform the following conversions: (i) (10111001.101) to Decimal and Hexadecimal (ii) (3AF.C) to Binary and Octal (iii) (726.4) to Binary and Decimal. b)Convert (13) to BCD, Excess-3, and Gray code.	6	CO1	L2
OR				
10	Simplify the Boolean function F(A,B,C,D) = Σm(0,1,2,5,8,9,10) using Karnaugh Map. Implement the simplified expression using NAND gates only.	6	CO1	L3
Module II				
11	Design a 4-bit binary parallel adder using full adders. Also explain the carry look-ahead adder and its advantage over ripple carry adder.	6	CO2	L3
OR				
12	Design a 2-bit magnitude comparator that compares two binary numbers A and B. Derive the logic expressions for A>B, A=B, and A<B.	6	CO2	L3
Module III				
13	Design a synchronous modulo-6 up counter using JK flip-flops. Give the state table, excitation table, and simplified logic expressions using K-map.	6	CO3	L3
OR				
14	Explain the operation of a Universal Shift Register with a block diagram. Show how it can be configured for: (i) Serial-in Serial-out (ii) Parallel-in Parallel-out (iii) Left shift and Right shift operations.	6	CO3	L3
Module IV				
15	Write Verilog HDL code for the following using structural and dataflow modelling: (i) 4-bit ripple carry adder (ii) 2-to-4 decoder (iii) 4-to-1 multiplexer. Simulate and write the test bench for any one circuit.	6	CO4	L3
OR				
16	With neat circuit diagrams, describe the working of: (i) CMOS inverter (ii) CMOS NAND gate (iii) CMOS NOR gate. Compare their power consumption characteristics with ECL family.	6	CO4	L2

25UAMT304	FUNDAMENTALS OF ARTIFICIAL INTELLIGENCE & DATA SCIENCE	Category	L	T	P	R	Credit	Year of Introduction
		ESC	3	1	0	0	4	2025

Preamble: Artificial Intelligence (AI) and Data Science are transformative technologies that are reshaping industries, economies, and everyday life across the globe. From intelligent virtual assistants and recommendation systems to autonomous vehicles and predictive healthcare analytics, AI and Data Science are driving innovation and enabling data-driven decision-making in unprecedented ways. The course provide students with a foundational understanding of the principles, methodologies, and applications of intelligent systems and data analytics.

Prerequisite: Nil

Course Outcomes: After the completion of the course, the student will be able to:

CO	Course Outcomes	Knowledge Level
CO1	Explain the concept of machine learning including neural networks and different learning techniques for engineering	K2 Understand

	applications.	
CO2	Apply mathematical concepts such as matrix operations, probability And regression to solve engineering problems.	**K3** Apply
CO3	Demonstrate knowledge of essential skills and tools required for Data Science, including data storage techniques and dataset creation.	**K3** Apply
CO4	Apply appropriate data pre-processing techniques to prepare datasets for analysis and modeling.	**K3** Apply

Mapping of course outcomes with program outcomes and program specific outcomes

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO 10**	**PO11**
CO1	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
CO2	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
CO3	**2**	**3**	**3**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
CO4	**3**	**3**	**3**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
Avg	**2.2**	**2.5**	**2.5**	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**

Mapping of course outcomes with Knowledge and Attitude Profile (WK)

	WK1	**WK2**	**WK3**	**WK4**	**WK5**	**WK6**	**WK7**	**WK8**	**WK9**
CO1	*	*	*	*	*				
CO2	*	*	*	*					
CO3		*	*	*	*				
CO4	*	*		*	*				

WKs Mapped with the course

WK1	**WK2**	**WK3**	**WK4**	**WK5**	**WK6**	**WK7**	**WK8**	**WK9**
*	*	*	*	*				

Mark Distribution:

Total Marks	**CIE Marks**	**ESE Marks**	**ESE Duration**

100	**40**	**60**	**2.5 hrs**

Continuous Internal Evaluation Pattern:

Attendance : 5 marks
Continuous Assessment Test : 20 marks
Continuous Assessment Assignment : 15 marks

SYLLABUS

Module 1 (14 hrs)

Basics of Machine Learning -types of Machine Learning systems-challenges in ML- Supervised learning model example- regression models- Classification model example- Logistic regression-unsupervised model example- K-means clustering. Artificial Neural Network- Perceptron- Universal Approximation Theorem.

Module 2 (14 hrs)

Role of linear algebra in Data representation and analysis – Matrix decomposition- Singular Value Decomposition (SVD)- Spectral decomposition. Basics of probability-random variables and statistical measures - rules in probability-Bayes theorem and its applications-Correlation analysis-linear correlation - regression analysis- linear regression.

Module 3 (14 hrs)

Data Science: Steps in doing Data Science - Data Science relation to other fields- Data Science and Information Science- Computational Thinking - Skills and tools needed to do Data Science - Storing data - Combining bytes into larger structures - Creating data sets - Identifying data problem - Understanding data sources - Exploring data models- Introduction to Big Data.

Module 4 (14 hrs)

Structured and unstructured data - Challenges with unstructured data - Data collection: Open data - multimodal data - Data Pre-processing: Data Cleaning - Data Integration, Data Transformation - Data Reduction - Data Discretization. Applications of Machine Learning in Data Science- modelling process- demonstration of ML. Benefits of data science-use of statistics and Machine Learning in Data Science- data science process applications in data science.

Text Books:

1. Gilbert Strang(2023), Introduction to Linear Algebra, Wellesley-Cambridge Press, 6th edition.

2. Gupta.S.C and V.K.Kapoor(2020) Fundamentals of mathematical statistics, Sultan Chand & Sons ,9th edition

3. Cielen, Davy and Arno Meysman(2016), Introducing data science: bigdata, machine learning, and more, using Python tools, Simon and Schuster, 1st edition

Reference Books:

1. Avrim Blum, John Hopcroft, and Ravi Kannan(2020) , Foundations of Data Science, Cambridge University Press, 1st edition
2. Carlos Fernandez(2017), Probability and Statistics for Data Science , Center for Data Science in NYU, 1st edition.
3. Kotu Vijay, and Bala Deshpande(2018) ,Data science: concepts and practice, Morgan 2nd edition

END SEMESTER EXAMINATION – MODEL QUESTION PAPER

Course Code: 25UAMT304	**Course Name: Fundamentals of Artificial Intelligence & Data Science**
Max. Marks: 60	**Duration: 2.5 Hours**

Part A (Answer all questions. Each question carries 3 marks)				
Qn No.	**Question**	**Marks**	**CO**	**BL**
1	Define machine learning and explain the difference between supervised and unsupervised learning with suitable examples.	3	CO1	L2
2	Explain the concept of Logistic Regression and state how it differs from Linear Regression.	3	CO1	L2
3	Define Singular Value Decomposition (SVD) and state its significance in data representation.	3	CO2	L2
4	State Bayes' theorem and explain its role in probability-based classification.	3	CO2	L2
5	List the essential skills and tools required to perform Data Science and explain any two in brief.	3	CO3	L2
6	Explain the concept of Computational Thinking and its relevance to Data Science.	3	CO3	L2
7	Define data pre-processing and explain the need for data cleaning in the data analysis pipeline.	3	CO4	L2
8	Distinguish between structured and unstructured data with suitable examples.	3	CO4	L2

Part B (Answer any one full question from each Module. Each carries 9 marks)				
Module I				
Qn No.	**Question**	**Marks**	**CO**	**BL**
9	Explain the different types of Machine Learning	9	CO1	L2

	systems in detail. Discuss the challenges involved in Machine Learning and illustrate how a supervised learning regression model works with an example.			
OR				
10	Describe the architecture and working principle of an Artificial Neural Network. Explain the Perceptron model and state the Universal Approximation Theorem with its significance in neural network design.	9	CO1	L2
Module II				
Qn No.	**Question**	**Marks**	**CO**	**BL**
11	A retail company has collected customer data represented as a matrix A consisting of 4 customers (rows) and 3 features: monthly spend, number of visits, and loyalty score (columns). The company wants to reduce the dimensionality of this data for visualization while preserving maximum variance. (a) Explain how Singular Value Decomposition (SVD) of matrix A can be used to achieve this dimensionality reduction. Outline the steps involved, including how the singular values indicate which components to retain. (b) A discrete random variable X represents the number of visits per month by a customer, with the following probability distribution: X = 1, 2, 3, 4 with P(X) = 0.1, 0.3, 0.4, 0.2 respectively. Calculate the mean (expected value) and variance of X, and interpret what these values tell the company about customer visiting behaviour.	9	CO2	L3
OR				
12	A medical testing centre uses a screening test for a disease that is present in 2% of the population. The test correctly identifies the disease in 95% of people who actually have it (true positive rate), and incorrectly indicates the disease in 4% of people who do not have it (false positive rate). A randomly selected person tests positive. (a) Apply Bayes' theorem to calculate the probability that this person actually has the disease. Comment on what this	9	CO2	L3

	result implies about the reliability of the test in practice. (b) The centre also recorded the age (X, in years) and blood pressure (Y, in mmHg) of 6 patients: X: 25, 32, 40, 48, 55, 60 Y: 118, 122, 130, 138, 145, 150 Calculate Pearson's correlation coefficient between age and blood pressure, and use simple linear regression to predict the blood pressure of a 50-year-old patient.			
Module III				
Qn No.	**Question**	**Marks**	**CO**	**BL**
13.a	A retail startup wants to build a system that predicts which products a customer will buy next, using past purchase records, website browsing logs, and social media reviews. Apply the steps involved in doing Data Science to outline how the team should proceed from problem identification to deployment, and justify how this process relates Data Science to other fields such as Information Science.	5	CO3	L3
13.b	A hospital wants to create a single dataset by combining numeric patient vitals, text-based doctor's notes, and X-ray images for analysis. Apply appropriate data storage techniques to combine these different types of bytes into larger structures, and identify the skills and tools the data science team would need to create this dataset.	4	CO3	L3
OR				
14.a	A telecom company is experiencing high customer churn but does not know the underlying cause. Apply the process of identifying the data problem and understanding the relevant data sources, such as call records, billing history, and complaint logs, that the company should investigate. Demonstrate with a suitable example how exploring different data models could help uncover patterns behind the churn.	5	CO3	L3
14.b	A social media platform generates millions of posts every day and wants to identify trending topics in real time. Apply the concept of Computational Thinking to decompose this problem into	4	CO3	L3

	manageable parts, and demonstrate the skills and tools needed to handle the Big Data characteristics, namely volume, velocity, and variety, involved in solving it.			
Module IV				
Qn No.	**Question**	**Marks**	**CO**	**BL**
15.a	Apply data pre-processing techniques—including Data Cleaning, Data Integration, Data Transformation, and Data Reduction—to prepare a given dataset for machine learning modeling. Explain Data Discretization with examples.	6	CO4	L3
15.b	Analyse how Machine Learning is applied in Data Science by describing the modelling process and the benefits of using statistics and Machine Learning in Data Science applications.	3	CO4	L3
OR				
16.a	Analyse the challenges involved in handling unstructured data. with the methods of data collection including open data and multimodal data, and apply appropriate pre-processing strategies for such data.	6	CO4	L3
16.b	Apply the data science process with real-world applications. Demonstrate how the use of statistics and Machine Learning contributes to data science process outcomes.	3	CO4	L3

25UHUT001	ECONOMICS FOR ENGINEERING PRACTICES	Category	L	T	P	R	Credit	Year of Introduction
		HMC	2	0	0	0	2	2025

Preamble: This syllabus covers the fundamentals of Microeconomics, Macroeconomics, and Engineering Economics. It bridges economic theory with practical engineering and management, teaching students to apply analytical tools to scarcity, market dynamics, and financial decision-making.

Prerequisite: Nil

Course Outcomes: After the completion of the course, the student will be able to:

CO	Course Outcomes	Knowledge Level
CO1	Understand the fundamentals of various economic issues using laws and learn the concepts of demand, supply, elasticity and production function.	K2 Understand
CO2	Develop decision making capability by applying concepts relating to costs and revenue, and acquire knowledge regarding the functioning of firms in different market situations.	K3 Apply
CO3	Outline the macroeconomic principles of monetary and fiscal systems and national income.	K2 Understand
CO4	Make use of the possibilities of value analysis and engineering, and take investment decisions through capital budgeting techniques.	K3 Apply

Mapping of course outcomes with program outcomes and program specific outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	**3**	**2**	**0**	**0**	**-**	**2**	**2**	**-**	**-**	**-**	**-**
CO2	**3**	**3**	**2**	**0**	**1**	**2**	**-**	**-**	**1**	**1**	**3**
CO3	**2**	**2**	**0**	**0**	**-**	**3**	**3**	**1**	**-**	**-**	**2**
CO4	**3**	**3**	**3**	**2**	**2**	**-**	**2**	**1**	**1**	**1**	**3**
Avg	**2.75**	**2.5**	**2.5**	**2**	**1.5**	**2.3**	**2.3**	**1**	**1**	**1**	**2.6**

Mapping of course outcomes with Knowledge and Attitude Profile (WK)

	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	*	*	*	*	*		*		*
CO2	*	*	*	*	*	*	*	*	
CO3	*	*	*	*	*		*	*	*
CO4	*	*	*	*	*	*		*	*

WKs Mapped with the course

WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
*	*	*	*	*	*	*	*	*

Mark Distribution:

Total Marks	CIE Marks	ESE Marks	ESE Duration
100	40	60	2.5 hrs

Continuous Internal Evaluation Pattern:

Attendance : 5 marks
Continuous Assessment Test : 20 marks
Continuous Assessment Assignment : 15 marks

SYLLABUS

Module 1 (7 hrs)

Nature and significance of economics, Basic economic problems – Production Possibility Curve – Utility – Law of diminishing marginal utility –Demand: Factors determining demand – Law of Demand – Demand curve- Price elasticity of demand- measurement of price elasticity and its applications – Supply: factors determining supply - Law of supply – Supply curve- Equilibrium price determination- Changes in demand and supply and its effects on equilibrium price and quantity. Production: Production function, Factors of Production- Cobb-Douglas Production Function

Module 2 (7 hrs)

Cost: Cost concepts – Private cost and social cost – Sunk cost – Opportunity cost -Explicit

and implicit cost –Short run cost curves –Long run average cost curve -Revenue concepts – Break-even point. Taxation-Direct and indirect taxes-principles of Taxation, GST.Market: Market: different market structures and market equilibrium – Kinked demand model- E-commerce, Stock market-SENSEX, NIFTY, Mutual Funds & ETFs (Concepts Only)

Module 3 (7 hrs)

National income: Concepts (GDP, GNP and NNP-Basic problems)– Final goods and Intermediate goods - Methods of Estimation –output method – expenditure method-- Difficulties in the measurement of national income. International trade, terms of Trade, Gain from International Trade, Free Trade vs. Protection**.** Dumping, and Balance of Payment. Inflation: Causes and Effects – Measures to Control Inflation - Monetary and Fiscal policies – Repo and reverse repo rate. Role of Science, Engineering and Technology In economic Development

Module 4 (7 hrs)

Value Analysis and value Engineering: Cost Value, Exchange Value, Use Value, Esteem Value - Aims, Advantages and Application areas of Value Engineering - Value Engineering Procedure.Capital Budgeting: Time value of money - Net Present Value Method - Benefit Cost Ratio – Internal Rate of Return -– Payback – Accounting Rate of Return.

Text Books:

1. Geetika, Piyali Ghosh and Chodhury, Managerial Economics, Tata McGraw Hill,2015
2. H. G. Thuesen, W. J. Fabrycky, Engineering Economy, PHI, 1966.
3. R. Paneerselvam: Engineering Economics, PHI, 2012.
4. I M Pandey, Financial Management, Vikas Publishing House ,2015

Reference Books:

1 Leland Blank P.E, Anthony Tarquin P. E., Engineering Economy Mc Graw Hill, 7th edition.

2. Khan M. Y, Indian Financial System, Tata McGraw Hill, 2011.

3. Donald G. Newman, Jerome P. Lavelle, Engineering Economics and analysis, Engg. Press, Texas, 2002.

4. Chan S. Park, Contemporary Engineering Economics, Prentice Hall of India Ltd, 2001.

5. Prasanna Chandra, Financial Management: Theory and Practice, Mc Graw Hill, 2007.

END SEMESTER EXAMINATION - MODEL QUESTION PAPER

Course Code	**25UHUT001**
Course Name	**ECONOMICS FOR ENGINEERING PRACTICES**
Max. Marks: 60	**Duration: 2.5 Hours**

Part A *(Answer all questions. Each question carries 3 marks)*				
Qn No.	**Question**	**Marks**	**CO**	**BL**
1	Explain is the Opportunity Cost principle	3	1	L2
2	Briefly explain the Cobb-Douglas Production Function	3	1	L2
3	Distinguish between Sunk Cost and Incremental Cost.	3	2	L2
4	Interpret the law of diminishing marginal utility using a real-world consumer scenario.	3	2	L3
5	Define Reverse Repo Rate and its impact on money supply.	3	3	L2
6	Define Exchange Value in Value Engineering?	3	3	L2
7	Explain the concept of Payback Period in project evaluation.	3	4	L2
8	Describe the financial meaning of the Internal Rate of Return (IRR) in capital budgeting decisions.	3	4	L3
Part B (*Answer any one full question from each Module. Each carries 9 marks*)				
Module 1				
Qn No.	Question	Marks	CO	
7(a)	Illustrate the Law of Diminishing Marginal Utility with a schedule and diagram.	5	1	L2
(b)	Explain the effect of an increase in Consumer Income on the equilibrium price and quantity of a normal good.	4	1	L2
OR				
8(a)	When the price of a machine part is ₹500, the supply is 100 units. When the price increases to ₹600, the supply rises to 150 units. Calculate the Price Elasticity of Supply and interpret the result.	5	1	L2

(b)	Discuss the three stages of the Law of Variable Proportions.	4	1	L2
MODULE-2				
9(a)	Compare the features of Perfect Competition and Monopoly markets.	5	2	L2
(b)	A firm has a Fixed Cost of ₹20,000 and a Variable Cost of ₹50 per unit. If the selling price is ₹100 per unit, calculate the Break-even Point in units.	4	2	L3
OR				
10(a)	Explain the Kinked Demand Curve model and why it leads to price rigidity in an Oligopoly.	5	2	L2
(b)	Differentiate between Private Cost and Social Cost using the example of industrial pollution.	4	2	L3
MODULE-3				
11(a)	Discuss the Difficulties in the Measurement of National Income in a developing economy.	5	3	L2
(b)	From the data given below estimate GNPmp, GNPfc and NNPmp and National income. GDPmp 5000(in 100 billion), NFIA = -50, indirect tax =70, subsidy =30, depreciation=30.	4	3	L2
OR				
12(a)	Explain Demand-Pull Inflation? Suggest two Fiscal Policy measures to control it.	5	3	L2
(b)	Explain the difference between Final Goods and Intermediate Goods with examples.	4	3	L2
MODULE-4				
13(a)	Describe the Aims and Advantages of applying Value Engineering in a construction project.	5	4	L3
(b)	Explain Use Value? How does it differ from Esteem Value?	4	4	L2
OR				
14(a)	An engineering project requires an initial investment of ₹5,000. The estimated annual cash inflows for 4 years are ₹2,000, ₹1,800, ₹1,600, and ₹1,400. If the discount rate is 8%, calculate the Net Present Value (NPV).	5	4	L3
(b)	State the decision rule for the Benefit-Cost Ratio (BCR) method.	4	4	L2

25UHUT002	SUSTAINABILITY AND ETHICS IN ENGINEERING	Category	L	T	P	R	Credit	Year of Introduction
		HMC	2	0	0	0	2	2025

Preamble: This course is designed to cultivate a holistic perspective in engineering students by integrating professional integrity, social equity, and environmental stewardship. In an era of rapid technological advancement and climate volatility, technical expertise alone is insufficient; the modern engineer must be a morally conscious decision-maker.

Prerequisite: Nil

Course Outcomes: After the completion of the course, the student will be able to:

CO	Course Outcomes	Knowledge Level
CO1	Explain fundamental ethical theories to resolve moral dilemmas in personal and professional contexts.	K2 (Understand)
CO2	Outline philosophical perspectives of environmental ethics to protect biodiversity and manage urban environmental impacts.	K2 (Understand)
CO3	Develop strategies for Zero Waste and Circular Economy to mitigate disruptions in the hydrological cycle and resource depletion.	K3 (Apply)
CO4	Illustrate the importance of Renewable Energy technologies in combating the climate crisis in relation to Environmental Regulations and the Sustainable Development Goals (SDGs).	K3 (Apply)

Mapping of course outcomes with program outcomes and program specific outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO1	-	-	-	-	-	2	-	3	2	2	-
CO2	-	-	-	-	-	3	-	2	3	2	-
CO3	1	1	2	-	-	2	3	-	-	-	-
CO4	2	2	3	2	2	2	3	1	-	2	2
Avg	**1.5**	**1.5**	**2.5**	**2**	**2**	**2.25**	**3**	**2**	**2.5**	**2**	**2**

Mapping of course outcomes with Knowledge and Attitude Profile (WK)

	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	*				*		*		
CO2	*				*		*		
CO3	*	*	*	*	*		*		*
CO4	*	*	*	*	*	*	*	*	*

WKs Mapped with the course

WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
*	*	*	*	*	*	*	*	*

Mark Distribution:

Total Marks	CIE Marks	ESE Marks	ESE Duration
100	40	60	2.5 hrs

Continuous Internal Evaluation Pattern:

Attendance : 5 marks
Continuous Assessment Test : 20 marks
Continuous Assessment Assignment : 15 marks

SYLLABUS

Module 1 (7 hrs)

Fundamentals of ethics -Moral Relativism vs. Objectivity. Consequentialism. Deontology Metaethics. Personal vs. professional ethics, Civic Virtue, Respect for others, Profession and Professionalism, Plagiarism, case studies, Technology and digital revolution, Cybertrust and cybersecurity, High technologies: connecting people and places- Managing conflict, Confidentiality, Codes of Ethics. Basic concepts in Gender Studies, gender, gender spectrum: gender stereotypes, Gender disparity and discrimination in education, Ethical values and practices in connection with gender Gender policy and women/transgender empowerment initiatives.

Module 2 (7 hrs)

Introduction to Environmental Ethics: key philosophical theories (anthropocentrism, biocentrism, ecocentrism).Deep Ecology.Intrinsic value.Sustainable Engineering Principles: Definition and scope, triple bottom line, life cycle analysis and

sustainability metrics. Ecosystems and Biodiversity: An overview of various ecosystems in Kerala/India, and its significance. Landscape and Urban Ecology: Principles of landscape ecology, Urbanization and its environmental impact, Moral Extensionism

Module 3 (7 hrs)

Hydrology and Water Management: water cycle, Environmental flow, disruptions and disasters. Zero Waste Concepts and Practices: Definition of zero waste and its principles, Strategies for waste reduction, Case studies of successful zero waste initiatives. Circular Economy and Degrowth: Differences between linear and circular economies, AI-Driven Energy Optimization**,** Digital Twins**,** Bio-Engineering & Biomimicry**,** Carbon Capture and Storage (CCS)**,** Mobility and Sustainable Transportation: Basic tenets of a Sustainable Transportation design, Integrated mobility systems, E-Mobility.

Module 4 (7 hrs)

Renewable Energy and Sustainable Technologies: (solar, wind, hydro, biomass), Challenges and opportunities in renewable energy adoption. Climate Change and Engineering Solutions: Kerala/India and the Climate crisis, Engineering solutions to mitigate, adapt and build resilience to climate change. Environmental Policies and Regulations: Ethical considerations in environmental policy-making. Case Studies and Future Directions: Analysis of real-world case studies, Emerging trends and future directions in environmental ethics and sustainability, Discussion on the role of engineers in promoting a sustainable future. The Sustainable Development Goal 17.

Text Books:

1. Whitbeck, C. (2011). Ethics in engineering practice and research (2nd ed.). Cambridge University Press.
2. Oakley, J. (2006). Virtue ethics and professional roles. Cambridge University Press.
3. Bakshi, B. R. (2019). Sustainable engineering: Principles and practice. Cambridge University Press.
4. Martin, M. W., & Schinzinger, R. (2014). Ethics in engineering (4th ed.). Tata McGraw-Hill Education.
5. Ahlawat, A. (2019). Sustainable development goals: Directive principles for sustainable India by 2030. Notion Press.

Reference Books:

1. Parmar, R. K. (2025). Green technology and sustainable development (1st ed.). ISBN-13 publication.
2. Kosanam, N. (2023). Beyond carbon: Responsible ways to restore ecological balance. ISBN-13 publication.

END SEMESTER EXAMINATION - MODEL QUESTION PAPER

Course Code	**25UHUT002**
Course Name	**SUSTAINABILITY AND ETHICS IN ENGINEERING**
Max. Marks: 60	**Duration: 2.5 Hours**

Part A *(Answer all questions. Each question carries 3 marks)*				
Qn No.	**Question**	**Marks**	**CO**	**BL**
1.	Differentiate between Moral Relativism and Objectivity in the context of professional decision-making.	3	1	L2
2.	Outline the key differences between personal ethics and professional ethics for a practicing engineer.	3	1	L2
3.	Explain the concept of 'Intrinsic Value' within environmental philosophy frameworks.	3	2	L2
4.	Summarise the three core pillars that constitute the 'Triple Bottom Line' of sustainability	3	2	L2
5.	Describe the engineering definition and operational importance of maintaining 'Environmental Flow' in river systems.	3	3	L2
6.	Differentiate between a Linear Economy and a Circular Economy using a conceptual pipeline breakdown.	3	3	L2
7.	Describe the challenges faced by coastal infrastructure in Kerala due to the ongoing climate crisis.	3	4	L2
8.	Outline the overarching objective of Sustainable Development Goal 17 regarding global partnerships.	3	4	L2
	Part B (*Answer any one full question from each Module. Each carry 9 marks*)			
	Module I			
Qn No.	**Question**	**Marks**	**CO**	**BL**
9	Describe the key principles of Consequentialism and Deontology. Explain their relevance in assessing a workplace confidentiality conflict in engineering	9	1	L2

	practice.			
	OR			
10	Explain the role of gender policies and empowerment initiatives in addressing structural discrimination within educational institutions.	9	1	L2
	Module II			
Qn No.	**Question**	**Marks**	**CO**	**BL**
11	Describe the key environmental philosophical theories of Anthropocentrism, Biocentrism, and Ecocentrism and their influence on modern industrial development policies.	9	2	L2
	OR			
12	Explain the key phases of Life Cycle Analysis (LCA) and the sustainability indicators used to evaluate the environmental performance of engineering products.	9	2	L2
	Module III			
Qn No.	**Question**	**Marks**	**CO**	**BL**
13.a	A town experiences frequent water shortages during summer. Apply the concepts of the water cycle and environmental flow to suggest suitable water management measures.	5	3	L3
13.b	Describe the concept of Carbon Capture and Storage (CCS) as a climate mitigation strategy. .	4	3	L2
	OR			
14.a	A residential colony generates a large amount of household waste. Apply the principles of Zero Waste to recommend two strategies for reducing waste generation.	5	3	L3
14.b	Explain the concept of AI-driven energy optimization and its significance in sustainable development.	4	3	L2
	Module IV			
Qn No.	**Question**	**Marks**	**CO**	**BL**
15.a	A coastal community is vulnerable to sea-level rise and flooding. Apply engineering solutions to improve its climate resilience.	5	4	L3
15.b	Summarize the opportunities and challenges	4	4	L2

	associated with renewable energy adoption in India.			
	OR			
16.a	A proposed industrial project is located near a sensitive ecosystem. Apply environmental policy and ethical principles to identify key considerations before project approval.	5	4	L3
16.b	Explain the importance of emerging sustainable technologies in achieving environmental sustainability.	4	4	L2

25UECL305	ELECTRONIC CIRCUITS – I LAB	Category	L	T	P	R	Credit	Year of Introduction
		PCL	0	0	3	0	2	2025

Preamble: The course familiarizes the students with the design, analysis, and practical implementation of analog electronic circuits using discrete components along with simulation-based verification of circuit behavior.

Prerequisite: Nil

Course Outcomes (COs): At the end of the course students should be able to:

CO	Course Outcomes	Knowledge Level
CO1	Apply circuit concepts to analyze wave shaping circuits, feedback circuits, and oscillators using discrete components.	K3 Apply
CO2	Apply the principles of amplifier and voltage regulator circuits to determine their performance parameters.	K3 Apply
CO3	Apply simulation tools to analyze wave shaping circuits, amplifiers, feedback circuits, and oscillators.	K3 Apply
CO4	Apply simulation tools to implement electronic circuits and determine their performance characteristics.	K3 Apply

CO- PO Mapping (Mapping of Course Outcomes with Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	3	2	2	-	-	-	3	3	-	3	3	2
CO2	3	3	3	2	-	-	-	3	3	-	3	3	3
CO3	3	3	2	2	3	-	-	3	3	-	3	3	2
CO4	3	3	3	2	3	-	-	3	3	-	3	3	3
Avg	3	3	2.5	2	3	-	-	3	3	-	3	3	2.5

Mapping of Course Outcomes with Knowledge and Attitude Profile (WK)

	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	*	*	*	*	*			*	
CO2	*	*	*	*	*			*	
CO3	*	*	*	*	*	*		*	
CO4	*	*	*	*	*	*		*	

WKs Mapped with the Course

WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
*	*	*	*	*	*		*	

Expt. No.	Experiments
	Part A – List of Experiments using discrete components **(Any *Six* experiments mandatory)**
1	RC Integrator and Differentiator - Study transient response and frequency response of RC integrating and differentiating circuits.
2	• Diode Clipping and Clamping Circuits - Study the operation and characteristics of clipping and clamping circuits.
3	• CE BJT Amplifier - Design a CE amplifier for a given voltage gain and plot its frequency response.
4	• CS MOSFET Amplifier - Design a CS MOSFET amplifier for a given voltage gain and plot its frequency response.
5	• Cascaded CE Amplifier - Design a two-stage CE amplifier and study gain and bandwidth.
6	• Cascode Amplifier - Design a cascode amplifier and study its frequency response.
7	• Feedback Amplifiers - Study current-series and voltage-series feedback amplifiers and their gain.
8	• RC Oscillator - Study RC phase shift or Wien bridge oscillator and measure frequency of oscillation.

9	• Class B and Class AB Power Amplifiers - Study operation and performance characteristics.
10	• Transistor Series Voltage Regulator - Design a voltage regulator and study load and line regulation with and without protection.

Part B – Simulation Experiments (Any *Six* experiments mandatory) The experiments shall be conducted using Open-Source Tools such as QUCS, KiCad, LT SPICE, or variants of SPICE tools.	
1	RC Integrator and Differentiator - Study transient response and frequency response of RC integrating and differentiating circuits.
2	Diode Clipping and Clamping Circuits - Study the operation and characteristics of clipping and clamping circuits.
3	CE BJT Amplifier - Design a CE amplifier for a given voltage gain and plot its frequency response.
4	CS MOSFET Amplifier - Design a CS MOSFET amplifier for a given voltage gain and plot its frequency response.
5	Cascaded CE Amplifier - Design a two-stage CE amplifier and study gain and bandwidth.
6	Cascode Amplifier - Design a cascode amplifier and study its frequency response.
7	Feedback Amplifiers - Study current-series and voltage-series feedback amplifiers and their gain.
8	RC Oscillator - Study RC phase shift or Wien bridge oscillator and measure frequency of oscillation.
9	Class B and Class AB Power Amplifiers - Study operation and performance characteristics.
10	Transistor Series Voltage Regulator - Design a voltage regulator and study load and line regulation with and without protection.

Course Assessment Method (CIE: 50 marks, ESE: 50 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Preparation/Pre-Lab Work experiments, Viva and Timely completion of Lab Reports / Record (Continuous Assessment)	Internal Examination	Total
5	25	20	50

End Semester Examination Marks (ESE):

Procedure/ Preparatory work/Design/ Algorithm	Conduct of experiment/ Execution of work/ troubleshooting/ Programming	Result with valid inference/ Quality of Output	Viva voce	Record	Total
10	15	10	10	5	50

Text Books:

- Boylestad, R. L., & Nashelsky, L. (2019). *Electronic devices and circuit theory* (12th ed.). Pearson.
- Sedra, A. S., Smith, K. C., Carusone, A. C., & Gaudet, V. (2020). *Microelectronic circuits* (8th ed.). Oxford University Press.
- Bogart, T. F., Beasley, J. S., & Rico, G. (2019). *Electronic devices and circuits* (7th ed.). Pearson.

Reference Books:

1. Razavi, B. (2015). *Fundamentals of microelectronics* (2nd ed.). Wiley.
2. Bell, D. A. (2008). *Electronic devices and circuits* (5th ed.). Oxford University Press.
3. Meganathan, D. (2023). *Electronic circuits: Analysis and design I* (1st ed.). Yes Dee Publishing.
4. Gopakumar, K. (2023). *Analysis and design of electronic circuits* (1st ed.). OWL Books.

25UECL306	DIGITAL LOGIC DESIGN LAB	Category	L	T	P		Credit	Year of Introduction
		PCL	0	0	3		2	2025

	WK1	WK2	WK3	WK4	WK5
CO1	*	*	*	*	*
CO2	*	*	*	*	*
CO3	*	*	*	*	*
CO4	*	*	*	*	*

Preamble: The Digital Electronics Laboratory provides practical exposure to the fundamental concepts and applications of digital systems, complementing theoretical knowledge through hands-on experiments and simulation. Using discrete components, integrated circuits, Verilog HDL, and FPGA platforms, students design, implement, and test combinational and sequential circuits. The laboratory enhances understanding of real-time digital system behavior and strengthens practical skills by bridging theory with implementation.

Prerequisite: Nil

Course Outcomes: After the completion of the course, the student will be able to:

CO	Course Outcomes	Knowledge Level
CO1	Apply the principles of combinational logic to construct digital circuits using integrated circuits (ICs) and verify their functionality.	K3 Apply
CO2	Apply the concepts of flip flops and counters to construct and verify sequential circuits using standard digital ICs	K3 Apply
CO3	Apply an industry-standard hardware description language (HDL) to implement digital circuits.	K3 Apply
CO4	Apply FPGA tools to implement digital circuits and interface them with external hardware components.	K3 Apply

Mapping of course outcomes with program outcomes and program specific outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	2	3	2	2	-	-	3	3	-	2	3	1
CO2	3	2	3	2	2	-	-	3	3	-	3	3	2
CO3	3	2	3	1	3	-	-	3	3	-	3	3	2
CO4	3	2	3	2	3	-	-	3	3	-	3	3	3
Avg	3	2	3	1.75	2.5	-	-	3	3	-	2.75	3	2

Mapping of course outcomes with Knowledge and Attitude Profile (WK)

WKs Mapped with the course

WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
*	*	*	*	*	*		*	

Mark Distribution:

Total Marks	CIE Marks	ESE Marks	ESE Duration
100	**50**	**50**	**3 hrs**

Continuous Internal Evaluation Pattern:

Attendance : 5 marks
Continuous Assessment : 25 marks
Internal Examination : 20 marks

End Semester Examination Marks (ESE):

Procedure/ Preparatory work/Design/ Algorithm	Conduct of experiment/ Execution of work/ troubleshooting/ Programming	Result with valid inference/ Quality of Output	Viva voce	Record	Total
10	**15**	**10**	**10**	**5**	**50**

SYLLABUS

Expt. No.	Experiments
	Part A – List of Experiments using digital components (Any *Six* experiments mandatory)
1	Design and Implementation of Boolean Functions Using Basic and Universal Logic Gates in SOP and POS Forms.
2	Design and Realization of half/full adder and subtractor using basic gates and universal gates.
3	Design and Implementation of 4-Bit Adder/Subtractor and BCD Adder Using IC 7483.
4	Study of Flip Flops : S-R, D, T, JK and Master slave JK FF using NAND gates
5	Implementation and Analysis of 3-Bit Asynchronous Up/Down Counter and Mod-N Counter.”
6	Construction and Verification of 4-Bit Synchronous Up/Down Counter and Mod-N Counter.
7	Ring counter and Johnson Counter.
8	Realization of counters using IC’s (7490, 7492, 7493).
9	Realization of combinational circuits using MUX & DEMUX, using ICs (74150, 74154)

10	Sequence Generator / Detector
Part B – Simulation Experiments (Any *Six* experiments mandatory) The experiments shall be conducted using Verilog and implementation using small FPGA	
1	Experiment 1: Familiarisation of Verilog HDL - Modelling of the basic gates using ● gate level modelling ● behavioural modelling ● structural modelling ● dataflow modelling
2	Experiment 2: Adders in Verilog (a) Development of verilog modules for half adder in any of the 3 modeling styles (b) Development of verilog modules for full adder in structural modeling using half adder.
3	Experiment 3: Mux and Demux in Verilog ● Development of verilog modules for a 4x1 MUX. (b) Development of verilog modules for a 1x4 DEMUX.
4	Experiment 4: Flipflops and counters (a) Development of verilog modules for SR, JK and D flipflops. (b) Development of verilog modules for a binary decade/Johnson/Ring counters
5	Experiment 5: Realization of Logic Gates and Familiarization of FPGAs ● Familiarization of a small FPGA board and its ports and interface. ● Create the .pcf files for your FPGA board. ● Familiarization of the basic syntax of verilog d) Development of verilog modules for basic gates, synthesis and implementation in the above FPGA to verify the truth tables.
6	Experiment 6. Multiplexer and Logic Implementation in FPGA (a) Make a gate level design of an 8 : 1 multiplexer, write to FPGA and test its functionality. (b) Use the above module to realize any logic function
7	Experiment 7. Flip-Flops and their Conversion in FPGA (a) Make gate level designs of J-K, J-K master-slave, T and D flip-flops, implement and test them on the FPGA board. (b) Implement and test the conversions such as T to D, D to T, J-K to T and J-K to D
8	Experiment 8: Asynchronous and Synchronous Counters in FPGA (a) Make a design of a 4-bit up down ripple counter using T-flip-flops in the previous

	experiment, implement and test them on the FPGA board. (b) Make a design of a 4-bit up down synchronous counter using T-flip-lops in the previous experiment, implement and test them on the FPGA board.
9	Experiment 10. BCD to Seven Segment Decoder in FPGA (a) Make a gate level design of a seven segment decoder, write to FPGA and test its functionality. (b) Test it with switches and seven segment display. Use ouput ports for connection to the display.
10	Experiment 8: Universal Shift Register in FPGA (a) Make a design of a 4-bit universal shift register using D-flip-flops in the previous experiment, implement and test them on the FPGA board. (b) Implement ring and Johnson counters with it.

Text Books:

- C. H. Roth, *Fundamentals of Logic Design*, 5th ed. Mumbai, India: Jaico Publishing House, 2009.
- B. J. LaMeres, *Introduction to Logic Circuits and Logic Design with Verilog*, 2nd ed. Cham, Switzerland: Springer International Publishing, 2017.
- J. Bhasker, *Verilog HDL Synthesis: A Practical Primer*. Hyderabad, India: B. S. Publications, 2001.

Reference Books

1. M. M. Mano and M. D. Ciletti, *Digital Design with an Introduction to Verilog HDL, VHDL, and SystemVerilog*, 6th ed. Harlow, U.K.: Pearson Education, 2018.
2. S. Palnitkar, *Verilog HDL: A Guide to Digital Design and Synthesis*, 2nd ed. Upper Saddle River, NJ, USA: Prentice Hall, 2003.
3. P. P. Chu, *FPGA Prototyping by Verilog Examples: Xilinx Spartan-3 Version*, 2nd ed. Hoboken, NJ, USA: Wiley, 2011.