

Wks Mapped with the course

WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
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Mark Distribution:

Total Marks	CIE Marks	ESE Marks	ESE Duration
100	40	60	2.5 hrs

Continuous Internal Evaluation Pattern:

Attendance	: 5 marks
Continuous Assessment Test	: 20 marks
Continuous Assessment Assignment	: 15 marks

SYLLABUS**Module 1 (12 hrs)**

Number Systems: Digital systems and binary numbers: number base conversions, octal/hexadecimal, complements, signed binary numbers. Binary Codes: BCD, Gray, Excess-3, and ASCII. Boolean Algebra: Basic definitions, postulates, and theorems; Boolean functions; standard and canonical forms (SOP and POS). Logic Gates: Standard gates (AND, OR, NOT, XOR, XNOR) and Universal gates (NAND, NOR); implementation of Boolean functions.

Module 2 (14 hrs)

Gate-Level Minimization: SOP/POS simplification using Karnaugh maps (up to 4 variables); don't care conditions; Quine-McCluskey (Tabulation) method for algorithmic simplification. Combinational Circuits: Design of Half/Full Adders and Subtractors; Parallel Adder; BCD Adder; Magnitude Comparator, Encoders, Decoders, Multiplexers, and Demultiplexers; Code converters.

Module 3 (15 hrs)

Flip-flops: SR, JK, T, and D flip-flops; level and edge triggering; truth tables, excitation tables, and characteristic equations; conversion between flip-flop types. Finite State Machines (FSM): Concept of State, Mealy and Moore Machines, Design of Sequence Detectors, State Diagrams and Tables. Counter design: Concept of counters; asynchronous (ripple) counters—binary up, binary down and BCD counters; synchronous counters—binary up, binary down, binary up/down counters, and BCD counters.

Module 4 (15 hrs)

Shift registers: Serial In Serial Out (SISO), Serial In Parallel Out (SIPO), Parallel In Parallel Out (PIPO), Parallel In Serial Out (PISO), bidirectional with parallel load. Specialized Counters: Ring counter, Johnson counter – timing sequences and state diagrams. Programmable logic: Programmable Logic Array (PLA), implementation of basic circuits using PLA. Verilog HDL: Introduction to HDL and basic concepts of Verilog; module structure, data types, operators, and modeling styles (gate-level, dataflow, behavioral). Design of simple combinational and sequential circuits using Verilog syntax; basic idea of test benches and simulation (theoretical only).

Text Books:

1. Mano, M. M. (2016). *Digital logic and computer design*. Pearson Education.
2. Floyd, T. L. (2017). *Digital fundamentals* (11th ed.). Pearson Education.
3. Palnitkar, S. (2003). *Verilog HDL: A guide to digital design and synthesis* (2nd ed.). Pearson.

Reference Books:

1. Mano, M. M., & Ciletti, M. D. (2018). *Digital design with an introduction to the Verilog HDL* (6th ed.). Pearson Education.
2. Givone, D. D. (2017). *Digital principles and design*. Tata McGraw Hill.
3. Wakerly, J. F. (2018). *Digital design: Principles and practices* (5th ed.). Pearson.

END SEMESTER EXAMINATION – MODEL QUESTION PAPER

Course Code	25UCST304
Course Name	SWITCHING THEORY AND LOGIC DESIGN
Max. Marks: 60	Duration: 2.5 Hours

Part A (Answer all questions. Each question carries 3 marks)				
Qn No.	Question	Marks	CO	BL
1.	Convert (245) ₁₀ to binary, octal, and hexadecimal. Also find the 1's and 2's complement of (10110101) ₂ .	3	CO1	L2
2.	Explain Gray code. Convert (13) ₁₀ to Gray code. Also convert (1011) _{Gray} to its decimal equivalent.	3	CO1	L2
3.	Simplify the Boolean function $F(A,B,C,D) = \sum m(0,1,2,5,8,9,10)$ using a Karnaugh map.	3	CO2	L3
4.	Design a full adder using basic logic gates. Also implement it using NAND gates only.	3	CO2	L3
5.	Explain the SR flip-flop with its truth table, characteristic equation, and excitation table. Convert it to a D flip-flop.	3	CO3	L2
6.	Design a 3-bit synchronous up counter. Draw the state diagram and state table.	3	CO3	L3
7.	Explain SISO and SIPO shift registers with timing diagrams. Give one application of each.	3	CO4	L2
8.	Write a Verilog behavioral model for a 2:1 multiplexer and describe its testbench.	3	CO4	L3

Part B (Answer any one full question from each Module. Each carry 9 marks)

Module I				
Qn No.	Question	Marks	CO	BL
9.1	Explain Boolean algebra postulates and theorems. Prove De Morgan's theorems. Simplify: $F = ABC + A'BC + AB'C + AB'C'$ using Boolean algebra.	5	CO1	L3
9.2	Explain BCD, Excess-3, and ASCII codes. Convert (2025) ₁₀ to BCD and Excess-3. Also show BCD addition: $7 + 8$.	4	CO1	L3
OR				
10.1	Implement the Boolean function $F(A,B,C) = \sum m(1,3,5,6,7)$ using: (i) AND-OR gates (SOP), (ii) OR-AND gates (POS), (iii) NAND gates only, and (iv) NOR gates only.	5	CO1	L3
10.2	Explain the working of NAND and NOR gates as universal gates. Implement a Full Subtractor using NAND gates only.	4	CO1	L3
Module II				
Qn No.	Question	Marks	CO	BL
11.1	Simplify $F(A,B,C,D) = \sum m(1,3,5,7,9,11,13,15)$ using the Quine-McCluskey (tabulation) method. Verify using a K-map.	5	CO2	L3
11.2	Design a 4-bit BCD adder. Show the correction logic needed when the sum exceeds 9.	4	CO2	L3
OR				
12.1	Design a 4-bit magnitude comparator that compares two 4-bit numbers A and B. Derive the logic expressions and draw the circuit.	5	CO2	L3
12.2	Implement a 4:1 multiplexer using basic gates. Use a 4:1 multiplexer to implement the Boolean function $F(A,B,C) = \sum m(0,2,5,7)$.	4	CO2	L3
Module III				
Qn No.	Question	Marks	CO	BL
13.1	Design a Mealy state machine for a sequence detector that detects the pattern '1011'. Draw the state diagram, state table, and obtain the next-state and output logic equations.	5	CO3	L3
13.2	Design a 4-bit synchronous BCD counter using JK flip-flops. Derive the flip-flop input equations and draw the logic circuit.	4	CO3	L3
OR				
14.1	Explain the conversion between flip-flop types. Convert a JK flip-flop to (i) D flip-flop and (ii) T flip-flop. Derive the conversion	5	CO3	L3

	logic.			
14. 2	Design a 3-bit asynchronous ripple counter. Explain its limitations compared to synchronous counters.	4	CO3	L3
Module IV				
Qn No.	Question	Marks	CO	BL
15. 1	Explain the Johnson counter and Ring counter. Draw their timing diagrams and state sequences for a 4-bit configuration. Compare their modulus counts.	5	CO4	L2
15. 2	Implement the Boolean functions $F1 = AB + AC$ and $F2 = A'B + BC'$ using a PLA. Show the PLA truth table and draw the PLA structure.	4	CO4	L3
OR				
16. 1	Explain Verilog HDL modeling styles: gate-level, dataflow, and behavioral. Write Verilog models for a 4-bit binary adder using all three styles.	5	CO4	L3
16. 2	Explain PIPO and PISO shift registers with diagrams and timing waveforms. Write a Verilog behavioral model for a 4-bit PISO shift register.	4	CO4	L3

