

CO3	*	*	*	*	*	*	*	*	*
CO4	*	*	*	*	*	*	*	*	*

Wks Mapped with the course

WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
*	*	*	*	*	*	*	*	*

Mark Distribution:

Total Marks	CIE Marks	ESE Marks	ESE Duration
100	50	50	3 hrs

Continuous Internal Evaluation Pattern:

Attendance : 5 marks

Preparation/Pre-Lab Work, Viva and Timely completion of Lab Reports : 25 marks

Internal Examination : 20 marks

SYLLABUS

PART A – Hardware Implementation

A1. *Study of digital trainer kit and basic digital ICs (7400 series). Verification of basic logic gates and Boolean theorems.

A2. Realization of basic logic gates using universal gates (NAND/NOR).

A3. Implementation of Half Adder and Full Adder (Breadboard).

A4. Implementation of Half Subtractor and Full Subtractor.

A5. Realization of a Boolean function in SOP and POS forms using basic gates.

A6. Implementation of 4:1 Multiplexer and 1:4 Demultiplexer.

A7. Implementation of 2-to-4 Decoder and 8-to-3 Encoder.

A8. Binary to Gray and Gray to Binary Code Converter.

PART B – Simulation Based Experiments

B1. Simulation and waveform verification of basic logic gates.

B2. Design and simulation of combinational circuits (Half/Full Adder, MUX/DEMUX, Encoder/Decoder).

B3. Design and simulation of a 2-bit magnitude comparator.

B4. Implementation of a Boolean function using MUX.

B5. Study of D flip flop and JK flip flops using ICs.

B6. Design and simulation of Shift Registers (SISO, SIPO, PISO, PIPO).

B7. Design and implement asynchronous counter – 3-bit up/down counter.

B8. Design and implement synchronous counter – 3-bit up/down counter, sequence generator.

PART C – Verilog HDL Based Implementation

C1. Modelling of basic logic gates (Gate-level, Dataflow, Behavioural modelling).

C2. Verilog implementation of Half Adder and Full Adder & Half Subtractor and Full Subtractor.

- C3. Verilog implementation of 4:1 MUX and 2-to-4 Decoder.
- C4. Verilog implementation of 8-to-3 Encoder and Code Converter.
- C5. Verilog design of 2-bit Magnitude Comparator.
- C6. Design and synthesize the behavioural model for a D flip flop in Verilog HDL.
- C7. Design and synthesize the behavioural model for a synchronous counter in Verilog.

Text Books:

- 1. Mano, M. M. (2020). Digital design (6th ed.). Pearson Education.
- 2. Leach, D. P., Malvino, A. P., & Saha, G. (2019). Digital principles and applications (10th ed.). McGraw-Hill Education.
- 3. Palnitkar, S. (2018). Verilog HDL: A guide to digital design and synthesis (2nd ed.). Prentice Hall.

Reference Books:

- 1. Roth, C. H., Jr., & Kinney, L. L. (2017). Fundamentals of logic design (7th ed.). Cengage Learning.
- 2. Brown, S., & Vranesic, Z. (2018). Fundamentals of digital logic with Verilog design (3rd ed.). McGraw-Hill Education.
- 3. Bhasker, J. (2019). A Verilog HDL primer (3rd ed.). Star Galaxy Publishing.