

25UCST40 2	COMPUTER ARCHITECTURE	Category	L	T	P	R	Credit	Year of Introduction
		PCC	4	0	0	0	4	2025

Preamble

The objective of this course is to enable learners to understand the fundamental architecture of a digital computer. It is essential for understanding the hardware behind the code and its execution at the physical level by interacting with memory and I/O structures. The course helps students understand computer system design to detect and solve problems occurring in computer architecture.

Prerequisite: 25UCST304 Switching Theory and Logic Design

Course Outcomes: After the completion of the course, the student will be able to:

CO	Course Outcomes	Knowledge Level
CO1	Identify the basic structure and functional units of a digital computer and the features of RISC and CISC architectures.	K2 Understand
CO2	Apply the design principles of single cycle processor in the design of the processor.	K3 Apply
CO3	Apply knowledge of arithmetic, logic circuits and the status register to design the Arithmetic Logic Unit (ALU).	K3 Apply
CO4	Explain organization of I/O and memory in a digital computer.	K2 Understand

Mapping of course outcomes with program outcomes and program specific outcomes

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	2	1	1	-	-	-	-	-	-	-	-	1	-
CO2	2	2	1	1	-	-	-	-	-	-	-	1	-
CO3	2	1	1	1	-	-	-	-	-	-	-	1	-
CO4	2	1	1	-	-	-	-	-	-	-	1	1	-
AVG	2	1.25	1	1	-	-	-	-	-	-	1	1	-

Mapping of course outcomes with Knowledge and Attitude Profile (WK)

	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	*	*	*	*	*			*	
CO2	*	*	*	*	*			*	
CO3	*	*	*	*	*			*	

CO4	*	*	*	*	*			*	
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Wks Mapped with the course

WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
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Mark Distribution:

Total Marks	CIE Marks	ESE Marks	ESE Duration
100	40	60	3 hrs

Continuous Internal Evaluation Pattern:

Attendance : 5 marks

Continuous Assessment Test : 20 marks

Continuous Assessment Assignment : 15 marks

SYLLABUS

Module 1 (14 hrs)

Basic Structure of computers: Functional units, basic operational concepts, and bus structures. Memory locations, addresses, and operations. CISC vs RISC architectures, RISC introduction, assembly language, and assembler directives. Programming concepts in RISC V: program flow, Branching, conditional statements, loops, functions, array declaration, Instruction execution cycle and addressing modes.

Module 2 (16 hrs)

Register transfer logic: inter-register transfer, arithmetic, logic, and shift micro-operations. Processor organization and ALU design: arithmetic circuits, logic circuits, status registers, shifters, and accumulators. Single-Cycle Processor: data path and control. Performance analysis.

Module 3 (13 hrs)

Pipelining: Basic principles, classification of pipeline processors, and instruction/arithmetic pipelines. Hazards: Structural, Data, and Control hazards; solving hazards and performance analysis. Arithmetic algorithms: Multiplication and division (restoring method), Array multiplier, and Booth's multiplication algorithm.

Module 4 (13 hrs)

I/O Organization: Accessing I/O devices, interrupts, and interrupt hardware. Direct Memory Access (DMA) and Embedded I/O systems. Memory system: Memory hierarchy, cache memories, and mapping functions. Cache replacement policies. Virtual memory: Address translation, page tables, and Translation Lookaside Buffer (TLB).

Text Books:

1. Hamacher, C., Vranesic, Z., Zaky, S., & Manjikian, N. (2011). Computer organization and embedded systems (6th ed.). McGraw-Hill.
2. Harris, S. L., & Harris, D. (2021). Digital design and computer architecture: RISC-V edition (2nd ed.). Morgan Kaufmann.
3. Mano, M. M., & Ciletti, M. D. (2017). Digital design (6th ed.). Pearson.

Reference Books:

1. Patterson, D. A., & Hennessy, J. L. (2021). Computer organization and design RISC-V edition (2nd ed.). Morgan Kaufmann.
2. Stallings, W. (2019). Computer organization and architecture: Designing for performance (11th ed.). Pearson.
3. Ledin, J. (2023). Modern computer architecture and organization (2nd ed.). Packt Publishing.

END SEMESTER EXAMINATION – MODEL QUESTION PAPER

Course Code	25UCST402
Course Name	COMPUTER ARCHITECTURE
Max. Marks: 60	Duration: 2.5 Hours

Part A (Answer all questions. Each question carries 3 marks)				
Qn No.	Question	Marks	CO	BL
1.	Differentiate RISC and CISC architectures. List the key features of RISC-V ISA.	3	CO1	L2
2.	Explain the instruction execution cycle with a neat diagram. What are the different addressing modes?	3	CO1	L2
3.	Design a 4-bit ripple carry adder using full adders and explain the carry propagation delay.	3	CO3	L3
4.	Explain the single-cycle processor data path. How are R-type and I-type instructions executed?	3	CO2	L2
5.	Multiply 13×11 using Booth's multiplication algorithm. Show all steps.	3	CO3	L3
6.	Explain structural, data, and control hazards in a pipeline. How can data hazards be resolved?	3	CO3	L2
7.	Explain direct mapping and set-associative mapping in cache memory with suitable examples.	3	CO4	L2
8.	Describe the working of DMA. Why is DMA preferred over interrupt-driven I/O for bulk data transfer?	3	CO4	L2

Part B

(Answer any one full question from each Module. Each carry 9 marks)				
Module I				
Qn No.	Question	Marks	CO	BL
9.a	Explain the basic structure of a computer with a neat block diagram showing all functional units and their interconnections.	5	CO1	L2
9.b	Write RISC-V assembly language programs for: (i) Computing factorial of a number, (ii) Swapping two numbers.	4	CO1	L3
OR				
10.a	Explain the bus structure of a computer. Differentiate between synchronous and asynchronous buses.	5	CO1	L2
10.b	Describe different types of micro-operations: arithmetic, logic, and shift micro-operations with examples.	4	CO1	L2
Module II				
Qn No.	Question	Marks	CO	BL
11	Design the ALU for a simple processor that supports ADD, SUB, AND, OR, and NOT operations. Show the data path and control signals for each operation.	9	CO3	L3
OR				
12.a	Illustrate the single-cycle processor control unit design. How are control signals generated for different instruction types?	5	CO2	L3
12.b	Perform CPI analysis for a processor executing a program with 40% ALU, 30% load/store, 20% branch, and 10% other instructions. Assume CPI for each type is 1, 2, 3, and 1 respectively.	4	CO2	L3
Module III				
Qn No.	Question	Marks	CO	BL
13	Explain the five-stage instruction pipeline. Describe how forwarding/bypassing resolves data hazards. Illustrate pipeline performance for a sequence of instructions with and without hazards.	9	CO3	L3
OR				
14.1	Divide 14 by 3 using the restoring division algorithm. Show all steps.	5	CO3	L3
14.2	Illustrate the Array multiplier circuit for two 4-bit numbers with a neat diagram.	4	CO3	L3

Module IV				
Qn No.	Question	Marks	CO	BL
15.1	Explain the virtual memory concept. Illustrate address translation using page tables and TLB.	5	CO4	L2
15.2	Compare LRU, FIFO, and Optimal page replacement policies with a suitable reference string example.	4	CO4	L2
OR				
16	Explain the memory hierarchy with a neat diagram. Illustrate cache memory organization and the different cache mapping techniques (Direct, Associative, Set-Associative) with examples.	9	CO4	L3
