

25UCST304	SWITCHING THEORY AND LOGIC DESIGN	Category	L	T	P	R	Credit	Year of Introduction
		ESC	3	1	0	0	4	2025

Preamble: The course introduces the fundamental concepts of digital systems, including number systems, binary codes, Boolean algebra, and logic gates. It develops the ability to analyze and design combinational and sequential circuits using systematic methods such as minimization techniques, flip-flops, counters, and state machines. The course also provides an introductory understanding of programmable logic and Verilog HDL for describing basic digital circuits. Upon completion, students will be able to design and analyze simple digital systems and understand their application in computer organization and digital electronics.

Prerequisite: Nil

Course Outcomes: After the completion of the course, the student will be able to:

CO	Course Outcomes	Knowledge Level
CO1	Explain the fundamentals of digital systems, number systems, binary codes, Boolean algebra, and logic gates.	K2 Understand
CO2	Apply Boolean algebra and minimization techniques to design and implement combinational logic circuits.	K3 Apply
CO3	Apply the principles of flip-flops, finite state machines, and counters to analyze and design sequential logic circuits.	K3 Apply
CO4	Develop shift registers, counters, and PLA-based designs, and describe them using basic Verilog HDL modeling concepts.	K3 Apply

Mapping of course outcomes with program outcomes and programme specific outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	1	1	1	-	-	-	-	-	-	1	3	1
CO2	3	3	3	2	-	-	-	-	-	-	1	3	2
CO3	3	3	3	2	-	-	-	-	-	-	1	3	2
CO4	3	3	3	2	2	-	-	-	-	-	2	3	3
Avg	3	2.5	2.5	1.75	2	-	-	-	-	-	1.25	3	2

Mapping of course outcomes with Knowledge and Attitude Profile (WK)

	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
--	-----	-----	-----	-----	-----	-----	-----	-----	-----

CO1	*	*	*	*	*			*	
CO2	*	*	*	*	*			*	
CO3	*	*	*	*	*			*	
CO4	*	*	*	*	*	*		*	

Wks Mapped with the course

WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
*	*	*	*	*	*		*	

Mark Distribution:

Total Marks	CIE Marks	ESE Marks	ESE Duration
100	40	60	2.5 hrs

Continuous Internal Evaluation Pattern:

Attendance	: 5 marks
Continuous Assessment Test	: 20 marks
Continuous Assessment Assignment	: 15 marks

SYLLABUS

Module 1 (12 hrs)

Number Systems: Digital systems and binary numbers: number base conversions, octal/hexadecimal, complements, signed binary numbers

Binary Codes: BCD, Gray, Excess-3, and ASCII.

Boolean Algebra: Basic definitions, postulates, and theorems; Boolean functions; standard and canonical forms (SOP and POS).

Logic Gates: Standard gates (AND, OR, NOT, XOR, XNOR) and Universal gates (NAND, NOR); implementation of Boolean functions.

Module 2 (14 hrs)

Gate-Level Minimization: SOP/POS simplification using Karnaugh maps (up to 4 variables); don't care conditions; Quine-McCluskey (Tabulation) method for algorithmic simplification.

Combinational Circuits: Design of Half/Full Adders and Subtractors; Parallel Adder; BCD Adder; Magnitude Comparator, Encoders, Decoders, Multiplexers, and Demultiplexers; Code converters.

Module 3 (15 hrs)

Flip-flops: SR, JK, T, and D flip-flops; level and edge triggering; truth tables, excitation tables, and characteristic equations; conversion between flip-flop types.

Finite State Machines (FSM): Concept of State, Mealy and Moore Machines, Design of Sequence Detectors, State Diagrams and Tables.

Counter design: Concept of counters; asynchronous (ripple) counters—binary up, binary down and BCD counters; synchronous counters—binary up, binary down, binary up/down counters, and BCD counters.

Module 4 (15 hrs)

Shift registers: Serial In Serial Out (SISO), Serial In Parallel Out (SIPO), Parallel In Parallel Out (PIPO), Parallel In Serial Out (PISO), bidirectional with parallel load.

Specialized Counters: Ring counter, Johnson counter – timing sequences and state diagrams.

Programmable logic: Programmable Logic Array (PLA), implementation of basic circuits using PLA.

Verilog HDL: Introduction to HDL and basic concepts of Verilog; module structure, data types, operators, and modeling styles (gate-level, dataflow, behavioral).

Design of simple combinational and sequential circuits using Verilog syntax; basic idea of test benches and simulation (theoretical only).

Text Books:

1. Mano, M. M. (2016). *Digital logic and computer design*. Pearson Education.
2. Floyd, T. L. (2017). *Digital fundamentals* (11th ed.). Pearson Education.
3. Palnitkar, S. (2003). *Verilog HDL: A guide to digital design and synthesis* (2nd ed.). Pearson.

Reference Books:

1. Mano, M. M., & Ciletti, M. D. (2018). *Digital design with an introduction to the Verilog HDL* (6th ed.). Pearson Education.
2. Givone, D. D. (2017). *Digital principles and design*. Tata McGraw Hill.
3. Wakerly, J. F. (2018). *Digital design: Principles and practices* (5th ed.). Pearson.

END SEMESTER EXAMINATION-MODEL QUESTION PAPER

Course Code	25UCST304
Course Name	SWITCHING THEORY AND LOGIC DESIGN
Max. Marks: 60	Duration: 2.5 Hours

	Part A <i>(Answer all questions. Each question carries 3 marks)</i>			
Qn No.	Question	Marks	CO	BL
1.	Describe Gray code and Excess-3 code. Explain their significance in digital systems with suitable examples.	3	1	L2
2.	Explain why NAND and NOR gates are called universal gates. Illustrate how a NOT gate can be implemented using a NAND gate or a NOR gate.	3	1	L2
3.	A digital display system must show a warning signal when exactly three out of four sensors are active. Apply Karnaugh map minimization to obtain a simplified Boolean expression for the control circuit.	3	2	L3
4.	A communication device receives a 4-bit Gray code input from a rotary encoder. Apply an appropriate code conversion technique to obtain the corresponding binary output.	3	2	L3

5.	A vending machine controller requires a memory element that changes state only on the triggering edge of a clock pulse to avoid false switching. Apply your knowledge of flip-flops to select a suitable flip-flop and justify your choice.	3	3	L3
6.	A security system must detect the input sequence "101" and generate an alarm signal whenever the sequence occurs. Apply the concept of finite state machines to identify whether a Mealy or Moore model would be more suitable and justify your answer.	3	3	L3
7.	A data acquisition system receives serial sensor data and must make the complete data word available simultaneously to a processor. Apply your knowledge of shift registers to select an appropriate register type and justify your choice.	3	4	L3
8.	A digital circuit designer wants to implement multiple combinational logic functions using a single programmable device instead of discrete gates. Apply the concept of Programmable Logic Arrays (PLA) to explain how this requirement can be achieved.	3	4	L3
Part B (Answer any one full question from each Module. Each carry 9 marks)				
Module I				
Qn No.	Question	Marks	CO	BL
9	Explain various binary codes used in digital systems, namely BCD, Gray, Excess-3, and ASCII. Compare their characteristics and discuss their applications in digital systems.	9	1	L2
OR				
10	Explain the fundamental postulates and theorems of Boolean algebra. Illustrate how Boolean functions can be represented using standard and canonical forms (SOP and POS) with suitable examples.	9	1	L2
Module II				
Qn No.	Question	Marks	CO	BL
11. a	A digital control system generates an output $F(A,B,C,D)$ that is HIGH for minterms 0, 2, 5, 7, 8, 10, 13, and 15. Apply Karnaugh map minimization to obtain the simplified SOP expression and realize the circuit using logic gates.	6	2	L3
11. b	A communication device must select one of four input channels for transmission over a single output line. Apply the concept of multiplexing to identify a suitable combinational circuit and explain its operation.	3	2	L3
OR				

12. a	A security system compares a 4-bit access code entered by a user with a stored reference code. Apply the concept of magnitude comparators to design a circuit that indicates whether the entered code is equal to, greater than, or less than the stored code.	6	2	L3
12. b	A factory automation system receives inputs from eight sensors but only one sensor can be active at a time. Apply the concept of an encoder to determine how the sensor information can be transmitted using fewer output lines.	3	2	L3
Module III				
Qn No.	Question	Marks	CO	BL
13. a	A traffic signal controller requires a memory element that toggles its state whenever a clock pulse arrives. Apply your knowledge of flip-flops to select a suitable flip-flop and explain its operation in this application.	5	3	L3
13.b	An event monitoring system needs a counter that counts from 0 to 7 repeatedly using minimum hardware. Apply the concept of asynchronous counters to design a suitable counter and explain its operation	4	3	L3
OR				
14. a	A parking management system must count the number of vehicles entering and leaving a parking lot. Apply the concept of a synchronous up/down counter to explain how the system can maintain the current vehicle count.	5	3	L3
14. b	A communication receiver must detect the bit sequence "1011" in a serial data stream and generate an output whenever the sequence occurs. Apply the concept of finite state machines to develop a suitable sequence detector.	4	3	L3
Module IV				
Qn No.	Question	Marks	CO	BL
15	A manufacturing plant requires a controller to activate four machines sequentially in a cyclic manner with minimal decoding circuitry. Apply the concepts of Ring and Johnson counters to develop a suitable solution and compare their operation for this application.	9	4	L3
OR				
16	A digital system designer needs to implement a 4-to-1 multiplexer for an FPGA-based application. Apply Verilog HDL to develop the module using an appropriate modeling style and explain the role of simulation in verifying the design.	9	4	L3