

25UCSL405	LOGIC SYSTEMS LAB	Category	L	T	P	R	Credit	Year of Introduction
		PCL	0	0	3	0	2	2025

Preamble: The Logic Systems Lab is designed to provide students with a comprehensive understanding of digital logic design through hands-on hardware implementation, circuit simulation, and hardware description language (HDL) based modeling. The course bridges the gap between theoretical concepts and practical realization of digital systems.

Prerequisite: 25UCST304 Switching Theory and Logic Design.

Course Outcome: -

After the completion of the course, the student will be able to:

CO	Course Outcomes	Knowledge Level
CO1	Construct and verify basic logic gates and combinational circuits using breadboard and digital trainer kit.	K3 Apply
CO2	Design and analyse digital circuits using circuit simulation software and interpret waveforms.	K3 Apply
CO3	Develop Verilog HDL modules and testbenches for combinational and simple sequential circuits.	K3 Apply
CO4	Correlate hardware implementation, simulation results and HDL realization of digital systems.	K4 Analyze

Mapping of course outcomes with program outcomes and programme specific outcomes

CO \ PO	PO1	PO2	PO3	PO4	PO5	PO 6	PO7	PO 8	PO 9	PO10	PO11	PSO1	PSO2
CO1	3	2	2	1	1	-	-	2	-	-	1	2	2
CO2	3	3	3	2	3	-	-	2	-	-	1	2	2
CO3	3	3	3	2	3	-	-	2	-	-	1	2	2
CO4	3	3	3	3	3	-	-	2	-	-	1	2	2
avg	3	2.75	2.75	2	2.5	-	-	2	-	-	1	2	2

Mapping of course outcomes with Knowledge and Attitude Profile (WK)

	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	*	*	*	*	*	*		*	
CO2	*	*	*	*	*	*		*	
CO3	*	*	*	*	*	*		*	
CO4	*	*	*	*	*	*		*	

Wks Mapped with the course

WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
*	*	*	*	*	*		*	

Course Assessment Method
(CIE: 50 marks, ESE: 50 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Preparation/Pre-Lab Work experiments, Viva and Timely completion of Lab Reports / Record (Continuous Assessment)	Internal Examination	Total
5	25	20	50

End Semester Examination Marks (ESE):

Procedure/ Preparatory work/ Design/ Algorithm	Conduct of experiment/ Execution of work/ troubleshooting/ Programming	Result with valid inference/ Quality of Output	Viva voce	Record	Total
10	15	10	10	5	50

- 1. Submission of Record: Students shall be allowed for the end semester examination only upon submitting the duly certified record.*
- 2. Endorsement by External Examiner: The external examiner shall endorse the record.*

Experiments

All HDL-based experiments should be done using Verilog HDL.

(Open-source simulation tools such as LTSpice/ Circuit Verse / Logisim Evolution or equivalent may be used.)

PART A – Hardware Implementation (Any Six Experiments with * as Mandatory)

(Introduction to digital design through breadboard wiring and basic combinational circuits.)

- A1. Study of digital trainer kit and basic digital ICs (7400 series). Verification of basic logic gates and Boolean theorems. *
- A2. Realization of basic logic gates using universal gates (NAND/NOR). *
- A3. Implementation of Half Adder and Full Adder (Breadboard).
- A4. Implementation of Half Subtractor and Full Subtractor.
- A5. Realization of a Boolean function in SOP and POS forms using basic gates. *
- A6. Implementation of 4:1 Multiplexer and 1:4 Demultiplexer.
- A7. Implementation of 2-to-4 Decoder and 8-to-3 Encoder.
- A8. Binary to Gray and Gray to Binary Code Converter. *

PART B – Simulation Based Experiments

(All experiments to be done using circuit simulation software.)

- B1. Simulation and waveform verification of basic logic gates.
- B2. Design and simulation of combinational circuits (any two):
 - 3. Half/Full Adder & Half/Full Subtractor
 - 4. Multiplexer / Demultiplexer
 - 5. Encoder / Decoder
- B3. Design and simulation of a 2-bit magnitude comparator.
- B4. Implementation of a Boolean function using MUX.
- B5. Study of D flip flop and JK flip flops using ICs
- B6. Design and simulation of Shift Registers performing SISO, SIPO, PISO & PIPO.
- B7. Design and implement an asynchronous counter - 3-bit up counter, 3-bit down counter
- B8. Design and implement a synchronous counter - 3-bit up counter, 3-bit down counter, sequence generator.

PART C – Verilog HDL Based Implementation

(All experiments in this part shall be implemented using Verilog HDL only.)

For each experiment:

- 6. Write Verilog program in IDE (Icarus Verilog / ModelSim / EDAPlayground or equivalent).
- 7. Develop appropriate testbench.
- 8. Simulate and verify waveforms.
 - C1. Modelling of basic logic gates using:(Any Two)
 - 1. Gate-level modelling
 - 2. Dataflow modelling
 - 3. Behavioural modelling
 - C2. Verilog implementation of Half Adder and Full Adder & Half Subtractor and Full Subtractor.
 - C3. Verilog implementation of 4:1 MUX and 2-to-4 Decoder.
 - C4. Verilog implementation of 8-to-3 Encoder and Code Converter.
 - C5. Verilog design of 2-bit Magnitude Comparator.
 - C6. Design and synthesize the behavioural model for a D flip flop in Verilog HDL
 - C7. Design and synthesize the behavioural model for a synchronous counter in Verilog

Text Books

1. Mano, M. M. (2020). *Digital design* (6th ed.). Pearson Education.
2. Leach, D. P., Malvino, A. P., & Saha, G. (2019). *Digital principles and applications* (10th ed.). McGraw-Hill Education.
3. Palnitkar, S. (2018). *Verilog HDL: A guide to digital design and synthesis* (2nd ed.). Prentice Hall.

Reference Books

1. Roth, C. H., Jr., & Kinney, L. L. (2017). *Fundamentals of logic design* (7th ed.). Cengage Learning.
2. Brown, S., & Vranesic, Z. (2018). *Fundamentals of digital logic with Verilog design* (3rd ed.). McGraw-Hill Education.
3. Bhasker, J. (2019). *A Verilog HDL primer* (3rd ed.). Star Galaxy Publishing.