

Mapping of course outcomes with Knowledge and Attitude Profile (WK)

	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	*	*	*	*	*				
CO2	*	*	*	*	*			*	
CO3	*	*	*	*	*			*	
CO4	*	*	*	*	*			*	

Wks Mapped with the course

WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
*	*	*	*	*			*	

Mark Distribution:

Total Marks	CIE Marks	ESE Marks	ESE Duration
100	40	60	3 hrs

Continuous Internal Evaluation Pattern:

Attendance : 5 marks
Continuous Assessment Test : 20 marks
Continuous Assessment Assignment : 15 marks

SYLLABUS**Module 1 (14 hrs)**

Basic Structure of computers: Functional units, basic operational concepts, and bus structures. Memory locations, addresses, and operations. CISC vs RISC architectures, RISC introduction, assembly language, and assembler directives. **Programming concepts in RISC V:** program flow, Branching, conditional statements, loops, functions, array declaration, Instruction execution cycle and addressing modes.

Module 2 (16 hrs)

Register transfer logic: inter-register transfer, arithmetic, logic, and shift micro-operations. **Processor organization and ALU design:** arithmetic circuits, logic circuits, status registers, shifters, and accumulators. Single-Cycle Processor: data path and control. Performance analysis.

Module 3 (13 hrs)

Pipelining: Basic principles, classification of pipeline processors, and instruction/arithmetic pipelines. **Hazards:** Structural, Data, and Control hazards; solving hazards and performance analysis. Arithmetic algorithms: Multiplication and division (restoring method), Array multiplier, and Booth's multiplication algorithm.

Module 4 (13 hrs)

I/O Organization: Accessing I/O devices, interrupts, and interrupt hardware. Direct Memory Access (DMA) and Embedded I/O systems. I/O storage methods. Memory system: Memory hierarchy, cache memories, and mapping functions. Cache replacement policies. Virtual memory: Address translation, page tables, and Translation Lookaside Buffer (TLB)

Text Books:

1. Hamacher, C., Vranesic, Z., Zaky, S., & Manjikian, N. (2011). *Computer organization and embedded systems* (6th ed.). McGraw-Hill.
2. Harris, S. L., & Harris, D. (2021). *Digital design and computer architecture: RISC-V edition* (2nd ed.). Morgan Kaufmann.
3. Mano, M. M., & Ciletti, M. D. (2017). *Digital design* (6th ed.). Pearson.

Reference Books:

4. Patterson, D. A., & Hennessy, J. L. (2021). *Computer organization and design RISC-V edition* (2nd ed.). Morgan Kaufmann.
5. Stallings, W. (2019). *Computer organization and architecture: Designing for performance* (11th ed.). Pearson.
6. Ledin, J. (2023). *Modern computer architecture and organization* (2nd ed.). Packt Publishing.

END SEMESTER EXAMINATION – MODEL QUESTION PAPER

Course Code	25UCST402
Course Name	COMPUTER ARCHITECTURE
Max. Marks: 60	Duration: 2.5 Hours

Part A (Answer all questions. Each question carries 3 marks)				
Qn No.	Question	Marks	CO	BL
1	Explain the functional units of a digital computer and briefly explain the role of each unit in program execution.	3	CO1	L2
2	Distinguish between RISC and CISC architectures with respect to instruction complexity and execution approach.	3	CO1	L2
3	Illustrate the instruction execution cycle with a suitable example, identifying the role of the data path at each stage.	3	CO2	L3
4	Apply the concept of register transfer notation to express an arithmetic micro-operation for two general-purpose registers.	3	CO2	L3
5	Apply Booth's algorithm to multiply two 4-bit signed binary numbers and show all intermediate steps.	3	CO3	L3

6	Solve the division of two 4-bit binary numbers using the restoring division method and verify the result.	3	CO3	L3
7	Describe the concept of cache memory and explain its role in the memory hierarchy.	3	CO4	L2
8	Explain the mechanism of Direct Memory Access (DMA) and identify the advantage it offers over interrupt-driven I/O.	3	CO4	L2
Part B <i>(Answer any one full question from each Module. Each carry 9 marks)</i>				
Module I				
Qn No.	Question	Marks	CO	BL
9	Explain the bus structure used to interconnect functional units and discuss how memory addresses and operations are organized in a stored-program computer.	9	1	L2
OR				
10	Explain the features of RISC architecture with suitable examples. Describe assembly language programming concepts in RISC-V including branching, conditional statements, loops, and function calls with array declaration.	9	1	L2
Module II				
Qn No.	Question	Marks	CO	BL
11	Illustrate the data path for a R type instruction and implement control unit design of RISC-V single-cycle processor	9	2	L3
OR				
12	Apply register transfer logic to design an Arithmetic Logic Unit (ALU) that supports arithmetic, logic, and shift micro-operations. Explain the role of the status register and accumulator in ALU operations.	9	2	L3
Module III				
Qn No.	Question	Marks	CO	BL
13.a	Demonstrate the operation of a pipelined processor by illustrating the execution of an instruction sequence through pipeline stages. Apply the concept of hazard resolution to solve a given pipeline scenario involving structural, data, and control hazards, and construct a modified pipeline timing diagram showing the effect of each hazard and its resolution technique.	5	3	L3
13.b	Construct the array multiplier circuit for the multiplication of two 4-bit binary numbers A = 1011 and B = 1101. Show all partial products, the arrangement of AND gates, and the carry-save adder network, and compute the final 8-bit product through the diagram.	4	3	L3

OR				
14.a	Apply Booth's multiplication algorithm to compute $A = 0110 \times B = 1101$ (4-bit signed 2's complement numbers). Construct the step-by-step operation table showing the accumulator, multiplier register, and control bit at each step, and verify the final 8-bit product by converting both operands to decimal.	5	3	L3
14.b	Apply the restoring division algorithm to divide the 8-bit dividend 00001101 (13) by the 4-bit divisor 0011 (3). Construct the step-by-step operation table showing the partial remainder, shift, subtract, and restore operations at each step, and verify the quotient and remainder by performing decimal multiplication.	4	3	L3
Module IV				
Qn No.	Question	Marks	CO	BL
15.a	Describe the memory hierarchy in a computer system. Explain direct mapping and set-associative mapping functions for cache memory and compare their performance using relevant examples.	6	4	L2
15.b	Explain the organization of embedded I/O systems and I/O storage methods used in modern computer architectures.	3	4	L2
OR				
16. a	Explain the concept of virtual memory. Describe address translation using page tables and outline the role of the Translation Lookaside Buffer (TLB) in improving translation speed.	6	4	L2
16.b	Explain the methods of accessing I/O devices in a computer system. Describe interrupt hardware and the steps involved in interrupt-driven I/O processing.	3	4	L2

