

25UECL306	DIGITAL LOGIC DESIGN LAB	Category	L	T	P		Credit	Year of Introduction
		PCL	0	0	3		2	2025

Preamble: The Digital Electronics Laboratory provides practical exposure to the fundamental concepts and applications of digital systems, complementing theoretical knowledge through hands-on experiments and simulation. Using discrete components, integrated circuits, Verilog HDL, and FPGA platforms, students design, implement, and test combinational and sequential circuits. The laboratory enhances understanding of real-time digital system behavior and strengthens practical skills by bridging theory with implementation.

Prerequisite: Nil

Course Outcomes: After the completion of the course, the student will be able to:

CO	Course Outcomes	Knowledge Level
CO1	Apply the principles of combinational logic to construct digital circuits using integrated circuits (ICs) and verify their functionality.	K3 Apply
CO2	Apply the concepts of flip flops and counters to construct and verify sequential circuits using standard digital ICs	K3 Apply
CO3	Apply an industry-standard hardware description language (HDL) to implement digital circuits.	K3 Apply
CO4	Apply FPGA tools to implement digital circuits and interface them with external hardware components.	K3 Apply

Mapping of course outcomes with program outcomes and program specific outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	2	3	2	2	-	-	3	3	-	2	3	1
CO2	3	2	3	2	2	-	-	3	3	-	3	3	2
CO3	3	2	3	1	3	-	-	3	3	-	3	3	2
CO4	3	2	3	2	3	-	-	3	3	-	3	3	3
Avg	3	2	3	1.75	2.5	-	-	3	3	-	2.75	3	2

	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	*	*	*	*	*	*		*	
CO2	*	*	*	*	*	*		*	
CO3	*	*	*	*	*	*		*	
CO4	*	*	*	*	*	*		*	

Mapping of course outcomes with Knowledge and Attitude Profile (WK)

Wks Mapped with the course

WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
*	*	*	*	*	*		*	

Mark Distribution:

Total Marks	CIE Marks	ESE Marks	ESE Duration
100	50	50	3 hrs

Continuous Internal Evaluation Pattern:

Attendance	: 5 marks
Continuous Assessment	: 25 marks
Internal Examination	: 20 marks

End Semester Examination Marks (ESE):

Procedure/ Preparatory work/Design/ Algorithm	Conduct of experiment/ Execution of work/ troubleshooting/ Programming	Result with valid inference/ Quality of Output	Viva voce	Record	Total
10	15	10	10	5	50

SYLLABUS

Expt. No.	Experiments

Part A – List of Experiments using digital components (Any <i>Six</i> experiments mandatory)	
1	Design and Implementation of Boolean Functions Using Basic and Universal Logic Gates in SOP and POS Forms.
2	Design and Realization of half/full adder and subtractor using basic gates and universal gates.
3	Design and Implementation of 4-Bit Adder/Subtractor and BCD Adder Using IC 7483.
4	Study of Flip Flops : S-R, D, T, JK and Master slave JK FF using NAND gates
5	Implementation and Analysis of 3-Bit Asynchronous Up/Down Counter and Mod-N Counter.”
6	Construction and Verification of 4-Bit Synchronous Up/Down Counter and Mod-N Counter.
7	Ring counter and Johnson Counter.
8	Realization of counters using IC’s (7490, 7492, 7493).
9	Realization of combinational circuits using MUX & DEMUX, using ICs (74150, 74154)
10	Sequence Generator / Detector
Part B – Simulation Experiments (Any <i>Six</i> experiments mandatory)	
The experiments shall be conducted using Verilog and implementation using small FPGA	
1	Experiment 1: Familiarisation of Verilog HDL - Modelling of the basic gates using ● gate level modelling ● behavioural modelling ● structural modelling ● dataflow modelling
2	Experiment 2: Adders in Verilog (a) Development of verilog modules for half adder in any of the 3 modeling styles (b) Development of verilog modules for full adder in structural modeling using half adder.
3	Experiment 3: Mux and Demux in Verilog ● Development of verilog modules for a 4x1 MUX. (b) Development of verilog modules for a 1x4 DEMUX.
4	Experiment 4: Flipflops and counters (a) Development of verilog modules for SR, JK and D flipflops. (b) Development of verilog modules for a binary decade/Johnson/Ring counters
5	Experiment 5: Realization of Logic Gates and Familiarization of FPGAs ● Familiarization of a small FPGA board and its ports and interface. ● Create the .pcf files for your FPGA board.

	Familiarization of the basic syntax of verilog d) Development of verilog modules for basic gates, synthesis and implementation in the above FPGA to verify the truth tables.
6	Experiment 6. Multiplexer and Logic Implementation in FPGA (a) Make a gate level design of an 8 : 1 multiplexer, write to FPGA and test its functionality. (b) Use the above module to realize any logic function
7	Experiment 7. Flip-Flops and their Conversion in FPGA (a) Make gate level designs of J-K, J-K master-slave, T and D flip-flops, implement and test them on the FPGA board. (b) Implement and test the conversions such as T to D, D to T, J-K to T and J-K to D
8	Experiment 8: Asynchronous and Synchronous Counters in FPGA (a) Make a design of a 4-bit up down ripple counter using T-flip-flops in the previous experiment, implement and test them on the FPGA board. (b) Make a design of a 4-bit up down synchronous counter using T-flip-flops in the previous experiment, implement and test them on the FPGA board.
9	Experiment 10. BCD to Seven Segment Decoder in FPGA (a) Make a gate level design of a seven segment decoder, write to FPGA and test its functionality. (b) Test it with switches and seven segment display. Use output ports for connection to the display.
10	Experiment 8: Universal Shift Register in FPGA (a) Make a design of a 4-bit universal shift register using D-flip-flops in the previous experiment, implement and test them on the FPGA board. (b) Implement ring and Johnson counters with it.

Text Books:

- C. H. Roth, *Fundamentals of Logic Design*, 5th ed. Mumbai, India: Jaico Publishing House, 2009.
- B. J. LaMeres, *Introduction to Logic Circuits and Logic Design with Verilog*, 2nd ed. Cham, Switzerland: Springer International Publishing, 2017.
- J. Bhasker, *Verilog HDL Synthesis: A Practical Primer*. Hyderabad, India: B. S. Publications, 2001.

Reference Books

- M. M. Mano and M. D. Ciletti, *Digital Design with an Introduction to Verilog HDL, VHDL, and SystemVerilog*, 6th ed. Harlow, U.K.: Pearson Education, 2018.
- S. Palnitkar, *Verilog HDL: A Guide to Digital Design and Synthesis*, 2nd ed. Upper Saddle River, NJ, USA: Prentice Hall, 2003.
- P. P. Chu, *FPGA Prototyping by Verilog Examples: Xilinx Spartan-3 Version*, 2nd ed. Hoboken, NJ, USA: Wiley, 2011.

