

Wks Mapped with the course

WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
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Mark Distribution:

Total Marks	CIE Marks	ESE Marks	ESE Duration
100	40	60	2.5 hrs

Continuous Internal Evaluation Pattern:

Attendance : 5 marks

Continuous Assessment Test : 20 marks

Continuous Assessment Assignment : 15 marks

SYLLABUS

Module 1 (16 Hrs)

Semiconductor Basics and Carrier Transport: Elemental and compound semiconductors, intrinsic and extrinsic semiconductors, effective mass, Fermi Dirac distribution, Fermi level, energy band diagrams, equilibrium and steady-state conditions, Excess carriers in semiconductors: Generation and recombination mechanisms of excess carriers, quasi Fermi levels.

Carrier concentration: Drift and diffusion mechanisms, mobility, conductivity, Hall effect and overview of transport equations. Einstein relations, Poisson equations, Continuity equations, Current flow equations, Diffusion length, Gradient of quasi Fermi level

Module 2 (15 Hrs)

PN Junctions and Bipolar Devices: PN junction formation, contact potential, electric field, charge distribution, biasing and Energy band diagrams, and ideal diode equation and characteristics.

Metal–semiconductor contacts. Electron affinity and work function,

Ohmic and Rectifying Contacts.

Bipolar junction transistor: operation, current components and base width modulation

Module 3 (15 Hrs)

MOS Capacitor and MOSFET Operation: MOS capacitor behavior in accumulation, depletion and inversion, threshold voltage and body effect. MOSFET: structure and types, basic drain current equations, drain and transfer characteristics.

Module 4 (10 Hrs)

MOSFET Scaling and Advanced Devices: Scaling concepts, sub-threshold conduction and short-channel effects.

Introduction to advanced devices such as MESFET and FinFET.

Text Books

1. Streetman, B. G., & Banerjee, S. K. (2010). *Solid state electronic devices* (6th ed.). Pearson Education.
2. Kang, S. M., & Leblebici, Y. (2002). *CMOS digital integrated circuits: Analysis and design* (3rd ed.). McGraw-Hill.
3. Pierret, R. F. (1996). *Semiconductor device fundamentals*. Addison-Wesley (Pearson Education).

Reference Books

1. Neamen, D. A. (2012). *Semiconductor physics and devices* (4th ed.). McGraw-Hill.
2. Sze, S. M., & Lee, M.-K. (2005). *Semiconductor devices: Physics and technology* (3rd ed.). John Wiley & Sons.
3. Pierret, R. F. (2006). *Semiconductor device fundamentals*. Pearson Education.
4. Sze, S. M. (2005). *Physics of semiconductor devices* (3rd ed.). John Wiley & Sons.

END SEMESTER EXAMINATION – MODEL QUESTION PAPER

Course Code	25UECT301
Course Name	SEMICONDUCTOR DEVICE TECHNOLOGY
Max. Marks: 60	Duration: 2.5 Hours

Part A (Answer all questions. Each question carries 3 marks)				
Qn No.	Question	Marks	CO	BL
1	Differentiate drift and diffusion movement of carriers in semiconductors.	3	1	L2
2	A solar-powered calculator manufacturer finds that pure silicon has low electrical conductivity. To improve device performance, engineers add impurity atoms to the silicon crystal. Apply the concept of doping to show how an intrinsic semiconductor is converted into an extrinsic semiconductor and how its conductivity is improved.	3	1	L3
3	Explain electron affinity and work function.	3	2	L2
4	An amplifier circuit used in a communication system	3	2	L3

	experiences variations in collector current when the collector-base voltage is increased, even though the base current is maintained constant. Apply the concept of the Early effect to illustrate why this occurs and explain its impact on the collector and base currents of the transistor.			
5	Explain the effect of real surfaces of a MOS capacitor.	3	3	L2
6	A power supply circuit uses a metal–n-type semiconductor junction to allow current flow in one direction while blocking it in the opposite direction. Apply the concept of a metal–semiconductor contact to illustrate the rectifying behaviour of the junction and explain how it controls current flow under forward and reverse bias conditions.	3	3	L3
7	Explain Drain induced barrier lowering.	3	4	L2
8	A semiconductor company is developing next-generation processors and requires transistors with better control over channel conduction and reduced leakage current than conventional MOSFETs. Illustrate how a FinFET structure addresses these requirements by drawing and explaining its structure and highlighting the role of the fin-shaped channel in improving device performance.	3	4	L3
Part B (Answer any one full question from each Module. Each carry 9 marks)				
Module I				
Qn No.	Question	Marks	CO	BL
9	Derive the expression for electron, hole and intrinsic concentrations at equilibrium in terms of effective density of states.	9	1	L3
OR				
10	Derive the expression for drift current density, mobility of carriers and conductivity of a semiconductor.	9	1	L3
Module II				
Qn No.	Question	Marks	CO	BL
11	Derive ideal diode equation with a neat sketch.	9	2	L3
OR				
12	Derive the expression for potential distribution of a PN junction at equilibrium.	9	2	L3
Module III				
Qn No.	Question	Marks	CO	BL
13. a	Derive the expression for drain current in linear and saturation region.	5	3	L3

13. b	In an electronics lab, engineers are testing an n-channel enhancement MOSFET used in an analog switching circuit. During analysis, they observe how the drain current varies with gate-source voltage in both linear and saturation regions. Apply this behaviour to illustrate the transfer characteristics of the MOSFET and show how it changes across linear and saturation regions.	4	3	L3
OR				
14. a	A silicon-based MOS capacitor used in a microelectronic sensor has a p-type substrate with doping concentration $N_A=10^{15}\text{cm}^{-3}$ and a gate oxide thickness of $100\text{ \AA}$. The device is operated at the onset of strong inversion for analysis of its switching behaviour. Determine: (i) Width of the depletion layer. (ii) Charge density in the depletion layer. (iii) Threshold voltage. Given $\epsilon_{\text{rox}}=3.9, \epsilon_{\text{rsi}}=11.8$.	5	3	L3
14. b	A silicon n-channel MOSFET used in an analog signal processing circuit is designed with an n^+ polysilicon gate and is operated under the conditions $V_{GS} = 3\text{ V}$, $V_{DS} = 5\text{ V}$, $V_T = 0.76\text{ V}$, $t_{\text{ox}} = 300\text{ \AA}$, $\mu_n = 600\text{ cm}^2/\text{Vs}$, $z = 50\text{ }\mu\text{m}$, $L = 10\text{ }\mu\text{m}$, and $C_{\text{ox}} = 1.15 \times 10^{-7}\text{ F/cm}^2$. Apply MOSFET current equations to determine the drain current under the given operating conditions.	4	3	L3
Module IV				
Qn No.	Question	Marks	CO	BL
15. a	A short-channel MOSFET used in a VLSI high-speed circuit shows performance degradation when operated at high drain voltage due to high-energy carriers near the drain region. Apply the concept of hot carrier effect to explain its impact on the performance and reliability of a short-channel MOSFET.	6	4	L3
15. b	A high-frequency communication system uses MESFET devices to achieve faster signal processing compared to conventional transistors. Engineers analyze its device behaviour to understand why it is suitable for microwave applications. Apply the concept of MESFET to explain its principle of operation, structure, and advantages in high-frequency applications.	3	4	L3
OR				
16. a	A MOSFET fabrication process is being optimized in semiconductor technology where device scaling is required to improve speed and packing density, and engineers compare constant field scaling with constant voltage scaling to understand their impact on device performance and reliability. Apply the concept of constant field scaling to explain its	6	4	L3

	principle and its advantages over constant voltage scaling.			
16. b	A MOSFET used in an analog integrated circuit shows a slight increase in drain current even after the device enters saturation, affecting the accuracy of circuit operation. Apply the concept of channel length modulation to explain its effect on the drain characteristics of the MOSFET.	3	4	L3