

25UECT303	DIGITAL LOGIC DESIGN	Category	L	T	P	R	Credit	Year of Introduction
		PBL	3	1	0	1	4	2025

Preamble: This course provides a strong foundation in digital electronics and digital system design, covering number systems, Boolean algebra, logic gates, and Karnaugh map simplification techniques. It focuses on the design and analysis of combinational and sequential circuits using standard digital components and finite state machine models. The course also introduces Verilog HDL for hardware modeling and implementation, and discusses logic families such as TTL, ECL, and CMOS with their characteristics and performance. Overall, it develops students' analytical, design, and practical skills for modern digital and embedded system applications..

Prerequisite: Nil

Course Outcomes: After the completion of the course, the student will be able to:

CO	Course Outcomes	Knowledge Level
CO1	Apply the knowledge of digital representation of information and Boolean algebra to deduce optimal digital circuits.	K3 Apply
CO2	Apply the principles of digital logic to construct combinational circuits such as adders, subtractors, multiplexers, decoders, and encoders.	K3 Apply
CO3	Apply the concepts of synchronous sequential circuits and finite state machines to solve complex digital system problems.	K3 Apply
CO4	Apply Verilog HDL to implement digital circuits and examine the characteristics of different logic families based on their electrical and performance parameters.	K3 Apply

Mapping of course outcomes with program outcomes and program specific outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	2	2	1	1	-	-	-	1	1	2	3	1
CO2	3	3	3	2	2	-	-	-	1	1	2	3	2
CO3	3	3	3	2	2	-	-	-	2	1	2	3	2
CO4	3	2	2	2	3	-	-	-	2	2	3	3	3
Avg	3.0	2.5	2.5	1.75	2.0	-	-	-	1.5	1.25	2.25	3.0	2.0

Mapping of course outcomes with Knowledge and Attitude Profile (WK)

	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
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CO1	*	*	*	*	*	*		*	
CO2	*	*	*	*	*	*		*	
CO3	*	*	*	*	*	*		*	
CO4	*	*	*	*	*	*		*	

Wks Mapped with the course

WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
*	*	*	*	*	*		*	

Mark Distribution:

Total Marks	CIE Marks	ESE Marks	ESE Duration
100	60	40	2.5 hrs

Continuous Internal Evaluation Pattern:

Attendance : 5 marks
 Continuous Assessment Test : 25 marks
 Project : 30 marks

Assessment and Evaluation for Project Activity

Sl. No	Evaluation for	Allotted Marks
1	Project Planning and Proposal	5
2	Contribution in Progress Presentations and Question Answer Sessions	4
3	Involvement in the project work and Team Work	3
4	Execution and Implementation	10
5	Final Presentations	5
6	Project Quality, Innovation and Creativity	3
	Total	30

Project Assessment and Evaluation criteria (30 Marks)

- Project Planning and Proposal (5 Marks)
 - Clarity and feasibility of the project plan
 - Research and background understanding

Defined objectives and methodology

2. Contribution in Progress Presentation and Question Answer Sessions (4 Marks)

Individual contribution to the presentation

Effectiveness in answering questions and handling feedback

3. Involvement in the Project Work and Team Work (3 Marks)

Active participation and individual contribution

Teamwork and collaboration

4. Execution and Implementation (10 Marks)

Adherence to the project timeline and milestones

Application of theoretical knowledge and problem-solving

Final Result

5. Final Presentation (5 Marks)

Quality and clarity of the overall presentation

Individual contribution to the presentation

Effectiveness in answering questions

6. Project Quality, Innovation, and Creativity (3 Marks)

Overall quality and technical excellence of the project

Innovation and originality in the project

Creativity in solutions and approaches

SYLLABUS

Module 1 (14 hrs)

Number Systems — Decimal, Binary, Octal, Hexadecimal, 1's and 2's complements, Codes — Binary, BCD, Excess 3, Gray, Alphanumeric codes, Boolean theorems, Logic gates, Universal gates, Sum of products and product of sums, Minterms and Maxterms, Karnaugh map Minimization

Module 2 (14 hrs)

Design of Half and Full Adders, Half and Full Subtractors, Binary Parallel Adder — Carry look ahead Adder, BCD Adder, Multiplexer, Demultiplexer, Magnitude Comparator, Decoder, Encoder, Priority Encoder.

Module 3 (14 hrs)

Flip flops — SR, JK, T, D, Master/Slave FF — operation and excitation tables, Triggering of FF, Analysis and design of clocked sequential circuits — Design — Moore/Mealy models, state minimization, state assignment, circuit implementation — Design of Counters- Ripple Counters, Ring Counters, Shift registers, Universal Shift Register.

Module 4 (14 hrs)

Introduction to Verilog HDL – Basic language elements, Basic implementation of logic gates and combinational circuits.

Logic Families: -Electrical characteristics of logic gates (Noise margin, Fan- in, Fan-out, Propagation delay, Transition time, Power -delay product) -TTL, ECL, CMOS. Circuit description and working of TTL and CMOS inverter, CMOS NAND and CMOS NOR gates.

Text Books:

1. M. M. Mano, *Digital Logic and Computer Design*, 4th ed. Noida, India: Pearson Education, 2013.
2. T. L. Floyd, *Digital Fundamentals*, 10th ed. Noida, India: Pearson Education, 2009.
3. S. Palnitkar, *Verilog HDL: A Guide to Digital Design and Synthesis*, 2nd ed. Noida, India: Pearson Education, 2003.

Reference Books:

1. M. M. Mano and M. D. Ciletti, *Digital Design with an Introduction to the Verilog HDL*, 5th ed. Noida, India: Pearson Education, 2013.
2. D. D. Givone, *Digital Principles and Design*. New Delhi, India: Tata McGraw-Hill, 2003.
3. J. F. Wakerly, *Digital Design: Principles and Practices*, 5th ed. Noida, India: Pearson Education, 2018.
4. A. Ananthakumar, *Fundamentals of Digital Circuits*, 4th ed. New Delhi, India: PHI Learning, 2016.

END SEMESTER EXAMINATION – MODEL QUESTION PAPER

Course Code	25UECT303
Course Name	DIGITAL LOGIC DESIGN
Max. Marks: 40	Duration: 2.5 Hours

Part A <i>(Answer all questions. Each question carries 2 marks)</i>				
Qn No.	Question	Marks	CO	BL
1	Convert $(245.75)_{10}$ to Binary, Octal, and Hexadecimal.	2	CO1	L2
2	State and prove De Morgan's theorems with truth table verification.	2	CO1	L2
3	Express the Boolean function $F(A,B,C) = \sum m(1,3,5,7)$ in canonical Sum	2	CO1	L3

	of Products (SOP) form and simplify using K-map.			
4	Design a half adder. Write the truth table and derive the logic expressions.	2	CO2	L3
5	Explain the operation of a JK Master-Slave Flip-Flop with a neat circuit diagram and timing diagram.	2	CO3	L2
6	Draw and explain a 4-bit ring counter using D flip-flops. Write the state sequence.	2	CO3	L2
7	Write a Verilog HDL module for a 2-to-1 multiplexer using data flow modelling.	2	CO4	L2
8	Define Fan-in, Fan-out and Noise Margin of logic gates. Why are these parameters important?	2	CO4	L2
Part B <i>(Answer any one full question from each Module. Each carries 6 marks)</i>				
Qn No.	Question	Marks	CO	BL
Module I				
9	a) Perform the following conversions: (i) $(10111001.101)_2$ to Decimal and Hexadecimal (ii) $(3AF.C)_{16}$ to Binary and Octal (iii) $(726.4)_8$ to Binary and Decimal. b) Convert $(13)_{10}$ to BCD, Excess-3, and Gray code.	6	CO1	L2
OR				
10	Simplify the Boolean function $F(A,B,C,D) = \sum m(0,1,2,5,8,9,10)$ using Karnaugh Map. Implement the simplified expression using NAND gates only.	6	CO1	L3
Module II				
11	Design a 4-bit binary parallel adder using full adders. Also explain the carry look-ahead adder and its advantage over ripple carry adder.	6	CO2	L3
OR				
12	Design a 2-bit magnitude comparator that compares two binary numbers A and B. Derive the logic expressions for $A > B$, $A = B$, and $A < B$.	6	CO2	L3
Module III				
13	Design a synchronous modulo-6 up counter using JK flip-flops. Give the state table, excitation table, and simplified logic expressions using K-map.	6	CO3	L3
OR				
14	Explain the operation of a Universal Shift Register with a block diagram. Show how it can be configured for: (i) Serial-in Serial-out (ii)	6	CO3	L3

	Parallel-in Parallel-out (iii) Left shift and Right shift operations.			
Module IV				
15	Write Verilog HDL code for the following using structural and dataflow modelling: (i) 4-bit ripple carry adder (ii) 2-to-4 decoder (iii) 4-to-1 multiplexer. Simulate and write the test bench for any one circuit.	6	CO4	L3
OR				
16	With neat circuit diagrams, describe the working of: (i) CMOS inverter (ii) CMOS NAND gate (iii) CMOS NOR gate. Compare their power consumption characteristics with ECL family.	6	CO4	L2