

25UECT415	DIGITAL SYSTEM DESIGN	Category	L	T	P	R	Credit	Year of Introduction
		PEC	2	1	0	0	3	2025

Preamble

This course provides a comprehensive foundation in the analysis and design of both asynchronous and clocked synchronous sequential circuits. It emphasizes the identification and mitigation of faults and hazards in digital systems to ensure reliable operation. The course also introduces modern hardware design methodologies through the use of Verilog and FPGA platforms, enabling students to design, implement, and validate practical digital systems aligned with current industry practices.

Pre-requisite: 25UECT303 Digital Logic Design

Course Outcomes:

After the completion of the course, the student will be able to:

Course Outcome		Knowledge Level
CO1	Demonstrate asynchronous and clocked synchronous sequential circuits	K3 Apply
CO2	Illustrate hazard-free digital circuits.	K3 Apply
CO3	Apply troubleshooting techniques to identify faults in digital circuits.	K3 Apply
CO4	Apply HDL programming in digital system design using FPGA	K3 Apply

Mapping of course outcomes with program outcomes and program specific outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	3	3	-	-	-	-	-	-	-	1	1	1
CO2	3	2	2	-	-	2	-	-	-	-	2	2	1
CO3	3	3	2	-	-	2	-	-	-	-	2	2	2
CO4	3	3	3	1	2	2	-	-	-	-	3	3	3
Avg	3	2.25	2.5	1	2	2	-	-	-	-	2	2	1.75

Mapping of course outcomes with Knowledge and Attitude Profile (WK)

	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	*	*	*	*	*		-	*	
CO2	*	*	*	*	*		*	*	
CO3	*	*	*	*	*		*	*	
CO4	*	*	*	*	*	*	*	*	

Wks Mapped with the course

WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
*	*	*	*	*	*	*	*	

Mark Distribution

Total Marks	CIE Marks	ESE Marks	ESE Duration
100	40	60	2.5 hrs

Continuous Internal Evaluation Pattern:

Attendance	: 5 marks
Continuous Assessment Test	: 20 marks
Continuous Assessment Assignment	: 15 marks

SYLLABUS**Module I (10 Hours)**

Introduction to clock-driven synchronous networks; analysis of clocked synchronous sequential circuits (CSSN); modeling techniques for CSSN; methods of state reduction and state assignment; and systematic design procedures for clocked synchronous sequential networks.

Module II (12 Hours)

Algorithmic State Machine (ASM) charts and their hardware realization; fundamentals of asynchronous sequential circuits; analysis techniques for asynchronous sequential circuits (ASC); methods of flow table reduction; race conditions in ASC and their resolution; state assignment challenges and formulation of transition tables.

Module III (10 Hours)

Static and dynamic hazards in combinational logic circuits; essential hazards and techniques for designing hazard-free circuits; data synchronizers and mixed-mode asynchronous circuit operation;

practical considerations including clock skew, clock jitter, and handling of synchronous and asynchronous inputs. Fault detection and analysis methods - fault table method, path sensitization technique, and Boolean difference method.

Module IV (10 Hours)

Introduction to FPGA architecture, including Look-Up Tables (LUTs), flip-flops, and routing resources; design entry using Hardware Description Languages (HDL); synthesis, implementation, timing verification, and generation of configuration bitstreams.

FPGA-based design methodology using industry tools, covering project setup, functional simulation, synthesis and implementation reports, analysis of resource utilization, and hardware testing/validation.

Text Books:

1. Givone, D. D. (2002). *Digital principles and design* (1st ed.). Tata McGraw-Hill.
2. Wakerly, J. F. (2008). *Digital design: Principles and practices* (4th ed.). Pearson Education.
3. Yarbrough, J. M. (2006). *Digital logic applications and design* (1st ed.). Cengage Learning India.
4. Abramovici, M., Breuer, M. A., & Friedman, A. D. (1994). *Digital systems testing and testable design*. John Wiley & Sons.
5. Pong P. Chu. (2017). *FPGA prototyping by System Verilog examples: Xilinx Micro Blaze MCS SoC* (2nd ed.). Wiley.

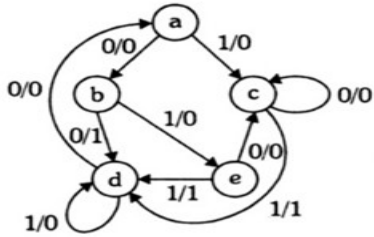
Reference Books:

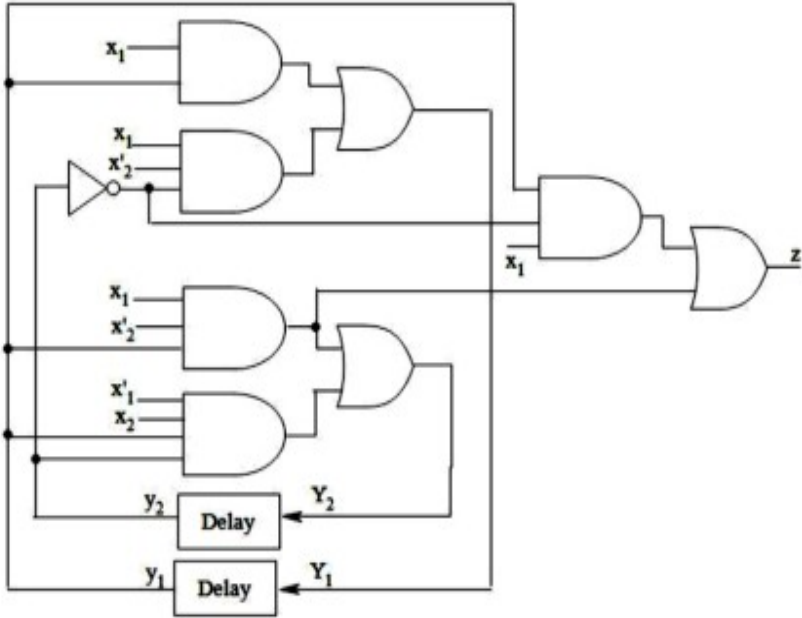
1. Biswas, N. N. (1992). *Logic design theory*. Prentice-Hall of India.
2. Haskell, R. E., & Hanna, D. M. (2009). *Introduction to digital design using Digilent FPGA boards*. LBE Books.
3. Palnitkar, S. (2003). *Verilog HDL: A guide to digital design and synthesis* (2nd ed.). Prentice Hall.
4. Yarbrough, J. M. (2006). *Digital logic applications and design* (1st ed.). Cengage Learning India.

END SEMESTER EXAMINATION – MODEL QUESTION PAPER

Course Code	25UECT415
Course Name	Digital System Design
Max. Marks: 60	Duration: 2.5 Hours

Part A <i>(Answer all questions. Each question carries 3 marks)</i>				
Qn No.	Question	Marks	CO	BL
1	A city traffic junction uses a clock-driven controller that changes signal states every 30 seconds in a fixed sequence. Explain why a	3	CO1	L3

	clock signal is essential in the operation of this synchronous sequential circuit. Identify the present state and next state concepts in this system.			
2	A washing machine operates through Wash → Rinse → Spin → Stop states. Explain the need of state assignment required before implementing the controller using flip-flops.	3	CO1	L3
3	An automatic parking gate opens only after verifying a valid RFID card. Develop the ASM chart of the system.	3	CO2	L3
4	A manufacturing controller contains six states, but analysis reveals that two states produce identical outputs and transitions. Explain how flow table reduction helps simplify the controller.	3	CO2	L2
5	Explain clock skew and its effects on synchronous circuits.	3	CO3	L2
6	Explain the steps in path sensitization method.	3	CO3	L2
7	Differentiate between signals and variables in VHDL.	3	CO4	L2
8	Explain structural modelling in VHDL programming.	3	CO4	L2
Part B (Answer any one full question from each Module. Each carries 9 marks)				
Qn No.	Question	Marks	CO	BL
Module I				
9.	A baggage handling system has eight operational states represented by a state table. After analysis, several states are found equivalent. Explain the state reduction method step-by-step and obtain a reduced-state machine. Discuss its impact on hardware complexity.	9	CO1	L3
OR				
	Apply the state reduction procedure to the given state diagram and obtain the reduced state machine. Clearly identify the equivalent states and draw the reduced state diagram. 	9	CO1	L3

Module II				
11.	Obtain a primitive flow table and a minimal row flow table for a fundamental-mode asynchronous sequential network meeting the following requirements: a. There are two inputs x_1 and x_2 and a single output z . b. The inputs x_1 and x_2 never change simultaneously. c. The output is to be 1 only when the values of x_1 and x_2 are both the same and x_2 was the variable that changed value causing x_1 and x_2 to become the same.	9	CO2	L3
OR				
12.	Analyze the asynchronous sequential network by forming the excitation/transition table, state table, flow table and flow diagram. The network operates in the fundamental mode with the restriction that only one input variable can change at a time. 	9	CO2	L3
Module III				
13.	Draw the logic diagram of the POS expression $Y = (x_1 + x_2')(x_2 + x_3)$. Show that there is a static-0 hazard when x_1 and x_3 are equal to 0 and x_2 goes from 0 to 1. Find a way to remove the hazard by adding one or more gates.	9	CO3	L3
OR				
14.	Illustrate the fault table method used for effective test set generation for the circuit $z = \bar{x}_1 x_2 + x_3$.	9	CO3	L3
Module IV				
15.	A digital system designer is implementing an Arithmetic Logic Unit (ALU) on an FPGA. One of the required modules is a 1-bit Full Adder	9	CO4	L3

	that will be integrated into a larger multi-bit arithmetic circuit. Develop a VHDL program for a 1-bit Full Adder and explain the functionality of the code. Illustrate how the design can be synthesized and verified using FPGA design tools.			
OR				
16.	A semiconductor company is developing a low-power FPGA-based smart sensor node for industrial automation. Before implementing the design on the target FPGA, the design team must follow a systematic VLSI design process starting from specification to hardware realization.	9	CO4	L3

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