

25UEET403	PULSE AND DIGITAL CIRCUITS	Category	L	T	P	R	Credit	Year of Introduction
		PBL	3	0	0	1	4	2025

Preamble: This course provides a strong foundation in digital electronics, focusing on combinational and sequential logic design techniques widely used in electrical and electronic systems. It introduces students to modern digital design practices through Hardware Description Language (Verilog) for combinational circuits, while emphasizing Finite State Machines (FSM) and Algorithmic State Machine (ASM) charts as systematic design tools for sequential systems. The course prepares students for advanced studies in digital systems, control, embedded systems and VLSI.

Prerequisite: IEE104 Introduction to Electrical & Electronics Engineering

Course Outcomes: After the completion of the course, the student will be able to:

CO	Course Outcomes	Knowledge Level
CO1	Explain number systems, Boolean algebra, logic gates and digital codes used in digital electronics.	K2 Understand
CO2	Apply the concept of Boolean algebra, Karnaugh maps and programmable logic devices to design combinational logic circuits.	K3 Apply
CO3	Implement and verify sequential logic circuits using flip-flops, registers, and counters.	K3 Apply
CO4	Illustrate basic ASM and FSM charts and implement simple combinational circuits using Verilog HDL.	K3 Apply

Mapping of course outcomes with program outcomes and program specific outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	1	1	1	-	-	-	-	-	-	1	3	1
CO2	3	3	3	2	-	-	-	-	-	-	1	3	2
CO3	3	3	3	2	-	-	-	-	-	-	1	3	2
CO4	3	2	2	2	3	-	-	-	-	-	2	3	2
Avg	3	2.25	2.25	1.75	3	-	-	-	-	-	1.25	3	1.75

Mapping of course outcomes with Knowledge and Attitude Profile (WK)

	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
CO1	*	*	*	*	*	-	-	*	-
CO2	*	*	*	*	*	-	-	*	-
CO3	*	*	*	*	*	-	-	*	-
CO4	*	*	*	*	*	*	-	*	-

Wks Mapped with the course

WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9
*	*	*	*	*	*	-	*	-

Mark Distribution:

Total Marks	CIE Marks	ESE Marks	ESE Duration
100	60	40	2 Hours

Continuous Internal Evaluation Pattern:

Attendance	: 5 marks
Continuous Assessment Test	: 25 marks
Mini Project	: 30 marks

SYLLABUS

Module 1 (16 Hours)

Digital number systems including binary, octal, and hexadecimal systems, base conversions, complements, and signed number representation. Digital codes including BCD, Gray code, and Excess-3 code and their applications. Boolean algebra postulates, laws, and theorems. Boolean expressions, canonical and standard forms, and simplification techniques. Logic gates including basic and universal gates and their implementation.

Module 2 (14 Hours)

Simplification of Boolean functions using algebraic method and Karnaugh maps up to four variables, including don't care conditions. Design and implementation of combinational circuits such as adders, subtractors, multiplexers, demultiplexers, encoders, decoders, comparators, code converters, and parity generator and checker circuits.

Introduction to programmable logic devices including ROM, PLA and PAL Introduction to FPGA architecture, logic blocks and interconnections and role of FPGA in modern digital system implementation.

Module 3 (14 Hours)

Concept of sequential circuits and memory elements. Latches and flip-flops including SR, JK, D, and T flip-flops, triggering methods, characteristic equations, and excitation tables. Flip-flop conversions and applications. Registers and shift registers including serial and parallel data transfer modes. Design and analysis of synchronous and asynchronous counters, timing diagrams and applications of counters in digital systems.

Module 4 (12 Hours)

Concept of finite state machines, state transitions, Moore and Mealy models, state diagrams, and state tables. Representation and design of sequential circuits using FSM.

Algorithmic State Machine (ASM) charts including ASM blocks, decision boxes, conditional output boxes and their use in digital system design.

Introduction to Hardware Description Language, need for HDL in digital design, structure of Verilog modules, ports and data types. Modelling of basic combinational circuits such as logic gates, multiplexers, adders and code converters using Verilog HDL.

Text Books

1. Mano, M. M. (2013). *Digital logic and computer design* (4th ed.). Pearson Education.
2. Floyd, T. L. (2009). *Digital fundamentals* (10th ed.). Pearson Education.
3. Palnitkar, S. (2003). *Verilog HDL: A guide to digital design and synthesis* (2nd ed.). Pearson Education.

Reference Books

1. Mano, M. M., & Ciletti, M. D. (2013). *Digital design with an introduction to Verilog HDL* (5th ed.). Pearson Education.
2. Wakerly, J. F. (2018). *Digital design: Principles and practices* (5th ed.). Pearson Education.
3. Roth, C. H., Kinney, L. L., & John, L. K. (2014). *Fundamentals of logic design* (7th ed.). Cengage Learning.
4. Brown, S., & Vranesic, Z. (2014). *Fundamentals of digital logic with Verilog design* (3rd ed.). McGraw-Hill Education.
5. Tocci, R. J., Widmer, N. S., & Moss, G. L. (2017). *Digital systems: Principles and applications* (12th ed.). Pearson Education.

Project-Based Learning Component

This course incorporates Project-Based Learning (PBL) to enable students to apply digital electronics concepts in the design and implementation of practical digital systems. Students shall identify a relevant digital system design problem based on electrical and electronic engineering applications and prepare a project proposal including problem statement, functional requirements, and design specifications.

Students shall design and develop appropriate solutions using combinational and sequential logic circuits, flip-flops, registers, counters the design shall be implemented using hardware components. The project shall be tested, validated, and demonstrated to verify its functionality and performance.

Suggested Project Topics

Project topics shall involve the design, simulation, and implementation of digital electronic systems such as:

1. Digital clock using counters and display interface
2. Traffic light controller
3. Digital frequency divider using flip-flops and counters
4. Digital voting machine
5. Digital code converter (Binary–Gray, Gray–Binary, BCD converter)
6. Digital lock system
7. LED pattern generator using shift registers
8. Digital alarm or event detection system using counters and logic circuits

Students may also propose other digital system design projects relevant to course outcomes, subject to approval by the course instructor.

Assessment and Evaluation of Project Activity

Sl. No.	Evaluation Component	Marks
1	Project Planning and Proposal	5
2	Progress Presentation and Technical Interaction	4
3	Participation and Team Work	3
4	Circuit Design, Execution, and Implementation	10
5	Final Demonstration and Presentation	5
6	Project Quality, Innovation, and Technical Merit	3
Total		30

Evaluation Guidelines

Project Planning and Proposal (5 Marks):

Assessment shall be based on clarity of problem definition, functional specifications, feasibility, and understanding of digital design concepts.

Progress Presentation and Technical Interaction (4 Marks):

Evaluation shall consider individual contribution, design understanding, and ability to explain design methodology and respond to questions.

Participation and Team Work (3 Marks):

Assessment shall be based on active involvement, collaboration, and individual responsibility in project activities.

Design, Simulation, and Implementation (10 Marks):

Evaluation shall consider correctness of logic design, simulation verification, HDL implementation (if applicable), hardware realization, and proper system operation.

Final Demonstration and Presentation (5 Marks):

Assessment shall be based on demonstration of working system, presentation quality, and technical clarity.

Project Quality, Innovation, and Technical Merit (3 Marks): Evaluation shall consider originality, complexity, innovation, and overall quality of digital system implementation.

END SEMESTER EXAMINATION – MODEL QUESTION PAPER
(STC 2025 SCHEME)

Course Code	25UEET403
Course Name	PULSE AND DIGITAL CIRCUITS
Max. Marks: 40	Duration: 2 Hours

Part A <i>(Answer all questions. Each question carries 2 marks)</i>				
Qn No.	Question	Marks	CO	BL
1	Convert the given decimal numbers to equivalent binary a) 125 b) 64	2	1	L2
2	Explain the implementation of NOT gate using NAND gate.	2	1	L2
3	Implement the function $F(A,B,C)=\Sigma(1,3,5,7)$ using a 4:1 multiplexer.	2	2	L3
4	Implement a half adder using basic logic gates and determine the outputs for all possible input combinations.	2	2	L3
5	A serial input 1101 is applied to a shift register. Determine the register contents after four clock pulses.	2	3	L3
6	Compare synchronous and asynchronous counters.	2	3	L2
7	Determine the output for $A=1, B=1$ and $C=0$ assign $Y = A ? (B \& C) : (B C)$;	2	4	L3
8	Compare Moore and Mealy machines.	2	4	L2
Part B <i>(Answer any one full question from each Module. Each carry 6 marks)</i>				
Module I				
Qn No.	Question	Marks	CO	BL
9.a.	Using Boolean laws, show that: $A'BC + ABC + AB'C = AC + A'BC$	3	1	L2
9.b.	Convert the following: a) Convert $(25)_{10}$ into binary. b) Convert $(101101)_2$ into decimal. c) Convert $(47)_{10}$ into BCD code. d) Convert $(1010)_2$ into Gray code. e) Convert Gray code $(1101)(1101)(1101)$ into binary.	3	1	L2

	f) Convert $(2F)_{16}$ into decimal.			
OR				
10.a	Convert the given function into canonical SOP form $F(A,B,C,D)=AB+CD$	3	1	L2
10.b	Convert the following: a) Convert $(94)_{10}$ into hexadecimal. b) Convert $(3A)_{16}$ into binary. c) Convert $(65)_{10}$ into BCD. d) Convert $(37)_{10}$ into Excess-3 code. e) Convert binary $(101101)_2$ into Gray code. f) Convert Gray code $(1110)(1110)(1110)$ into binary.	3	1	L2
Module II				
Qn No.	Question	Marks	CO	BL
11.a	Minimize the Boolean function using a 4-variable K-map, $F(A,B,C,D)=\Sigma(0,2,5,7,8,10,13,15)$	3	2	L3
11.b	A digital system performs addition and comparison of two binary numbers, $A=1010$ and $B=0111$ Determine: a) Sum using a parallel adder. b) Comparator outputs.	3	2	L3
OR				
12.	Implement the following functions using a PLA: $F_1(A,B,C)=\Sigma(1,3,5,7)$ $F_2(A,B,C)=\Sigma(0,2,4,6)$	3	2	L3
12.b	Minimize the following using a 4-variable K-map: $F(A,B,C,D)=\Sigma(0,2,4,6,8,10,12,14)$	3	2	L3
Module III				
Qn No.	Question	Marks	CO	BL
13.	Design a 4 bit down counter using JK flip flop	6	3	L3
OR				
14.	Design a MOD-10 asynchronous counter using JK flip-flops	6	3	L3

	and determine the counting sequence.			
Module IV				
Qn No.	Question	Marks	CO	BL
15.	Apply the Mealy model to detect the sequence 1101 and determine the state transitions and outputs	6	4	L3
OR				
16.	Develop the ASM chart for a traffic light controller having three states and determine the output conditions.	6	4	L3
